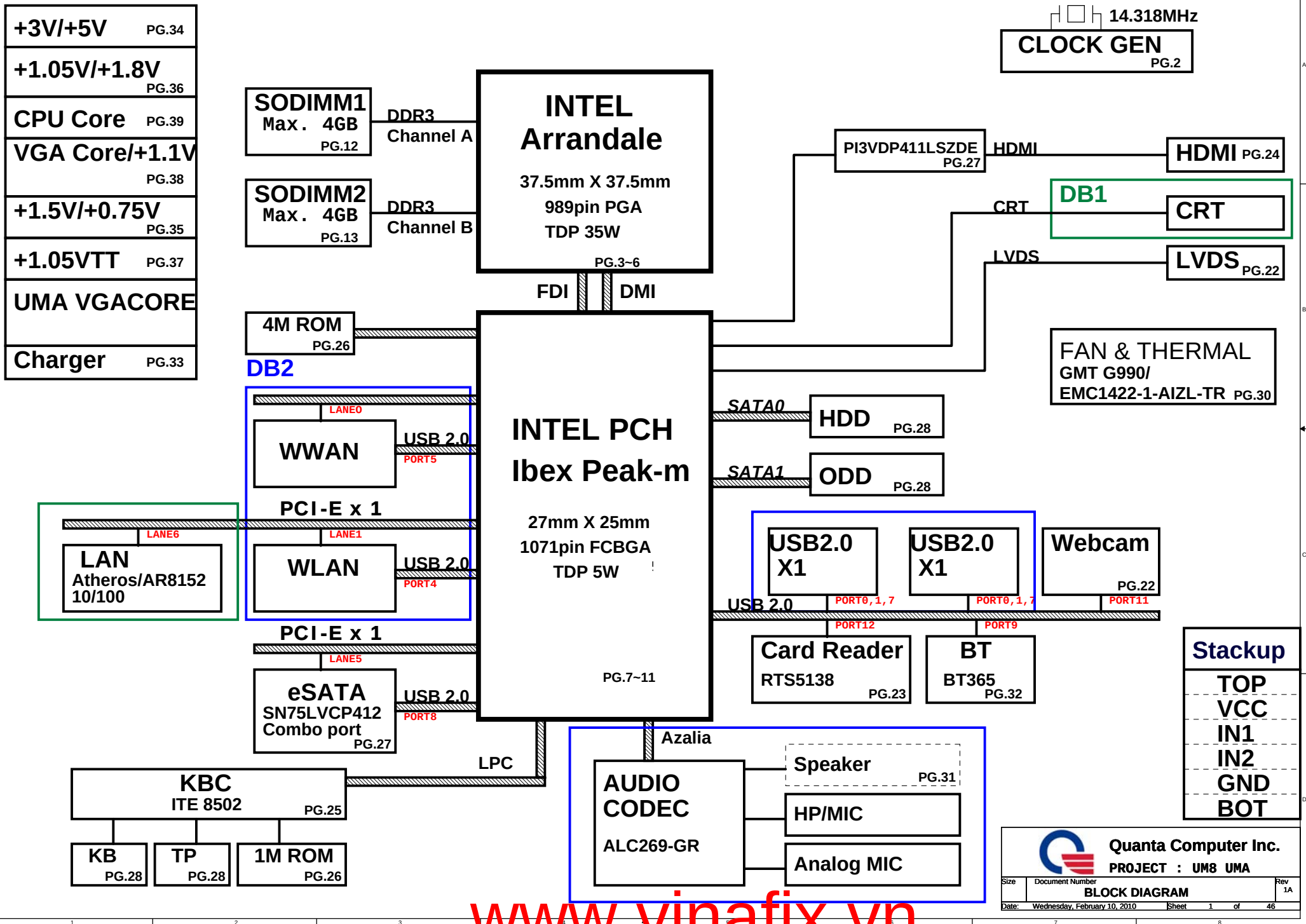
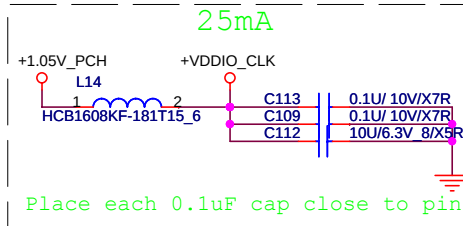
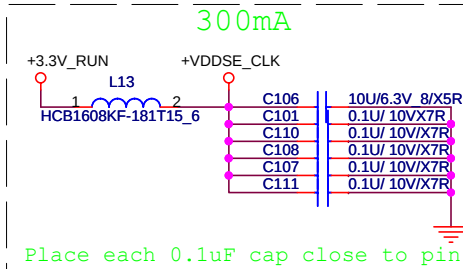


UM8 UMA SYSTEM DIAGRAM



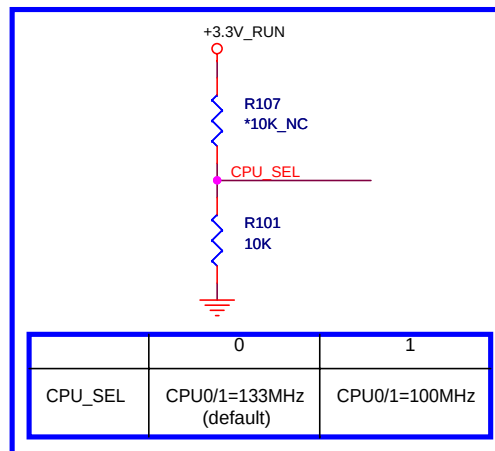
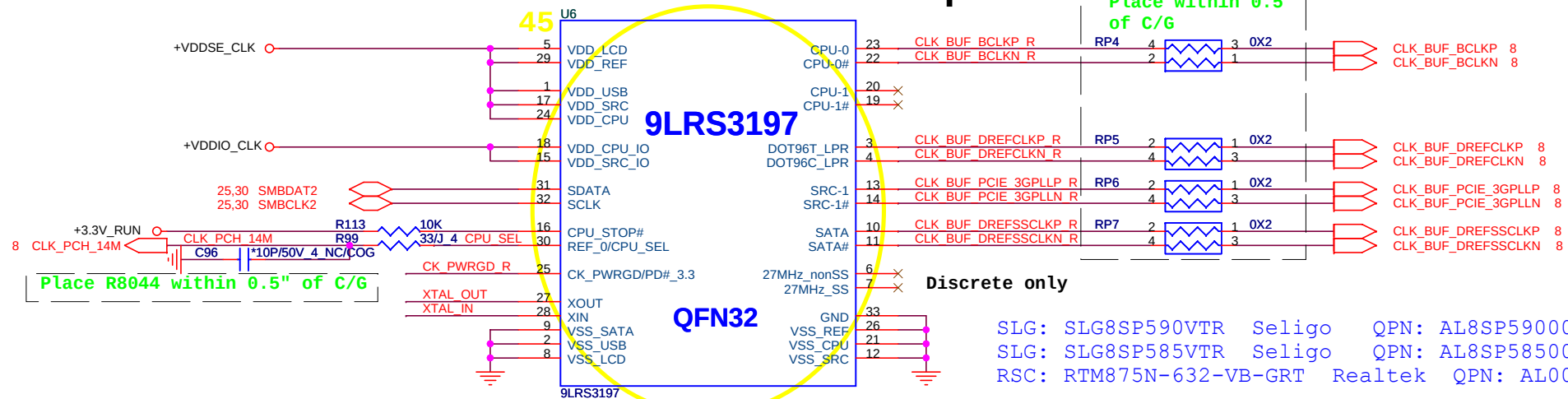


8/20 Wait Victor check

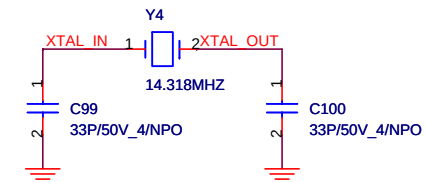
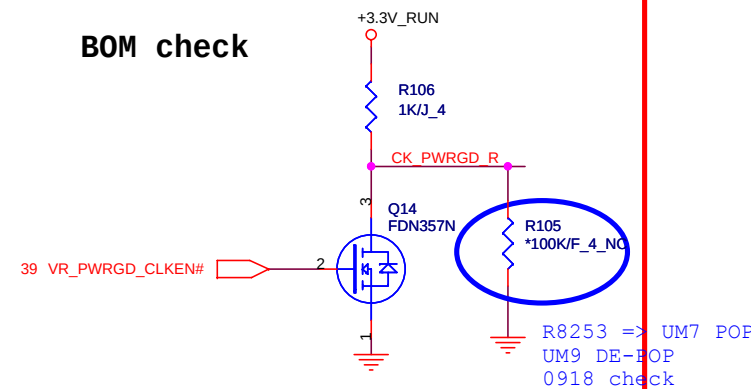


PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint



BOM check



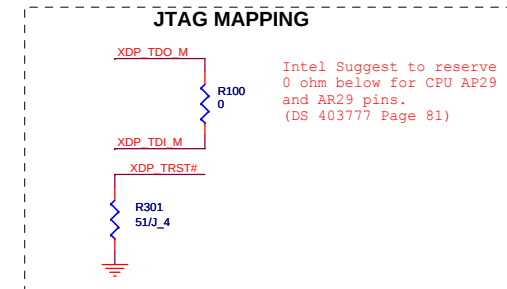
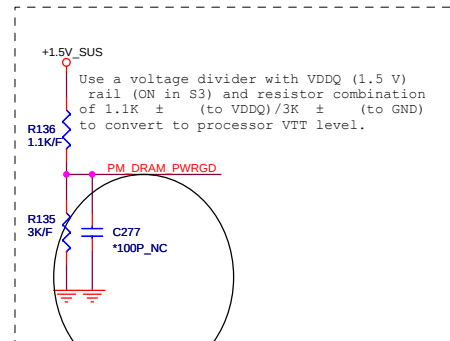
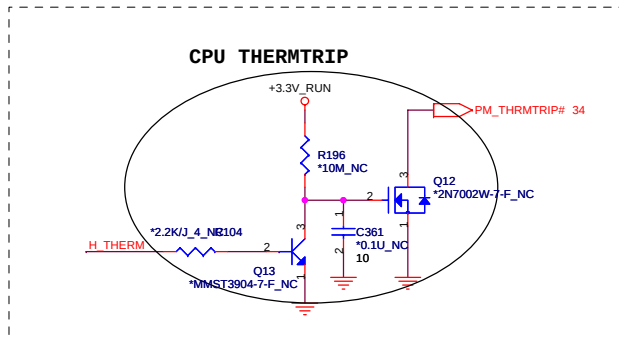
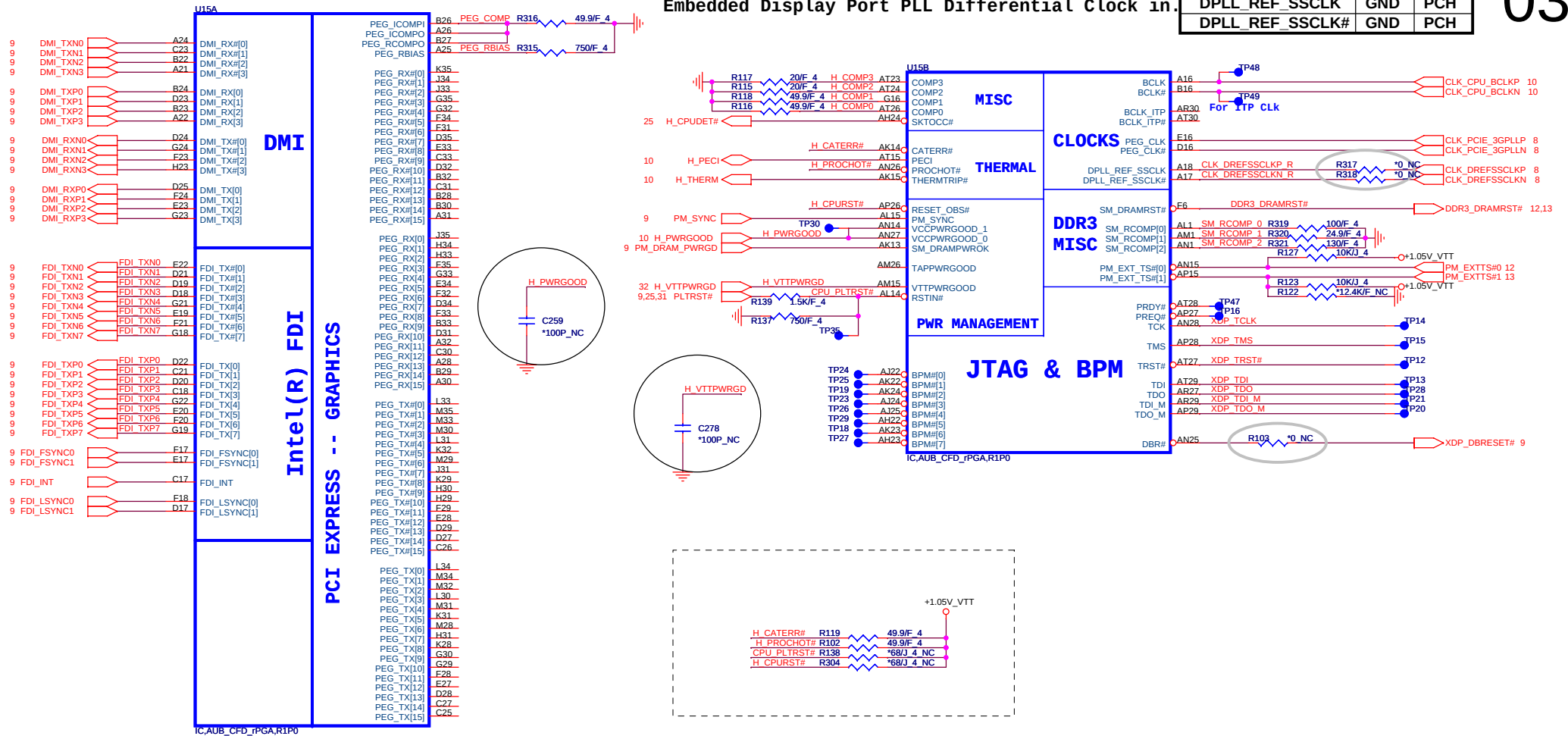
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Clock Gen(9LRS3197)/HOLES	Rev 1A
Date:	Wednesday, February 10, 2010	Sheet 2 of 46	

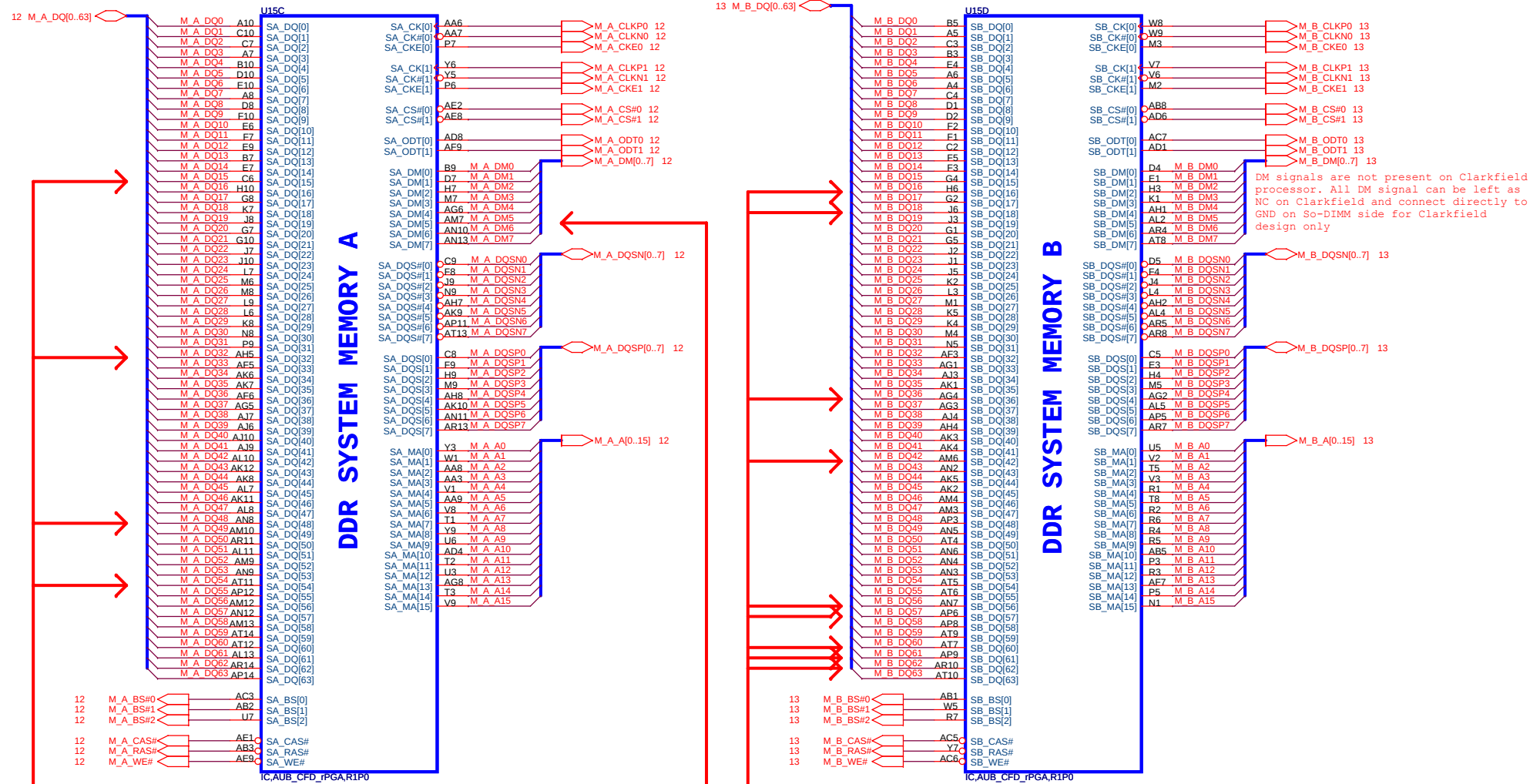
DPLL_REF_SSCLK/DPLL_REF_SSCLK#: Embedded Display Port PLL Differential Clock in.

DPLL_REF_SSCLK	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

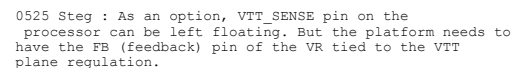


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

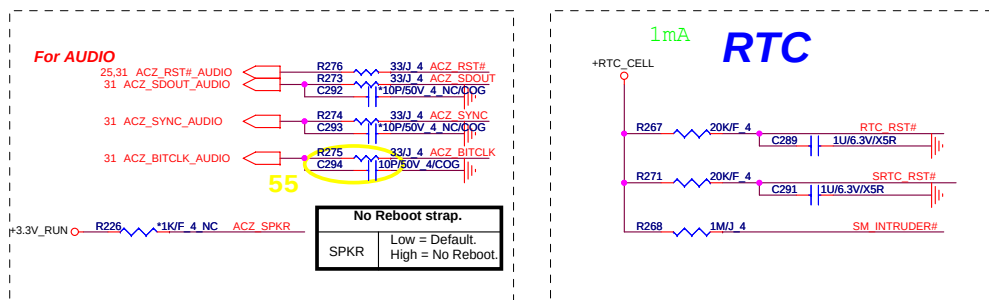
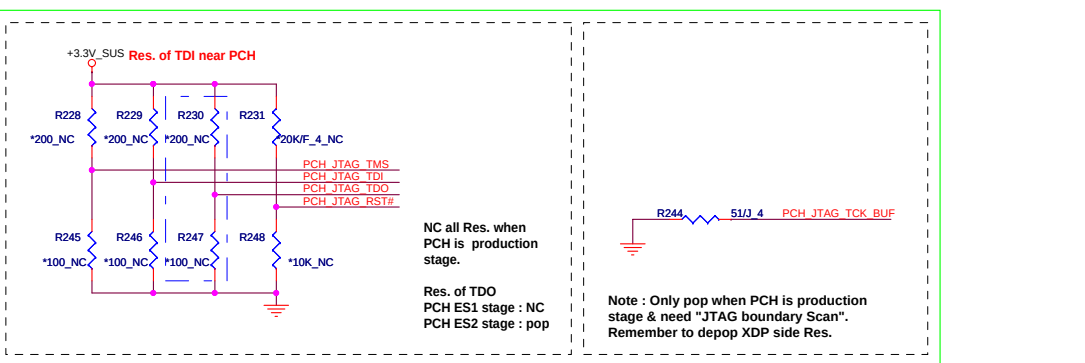
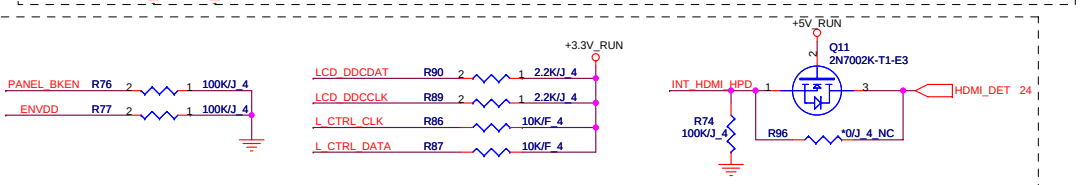
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



+VCC CORE

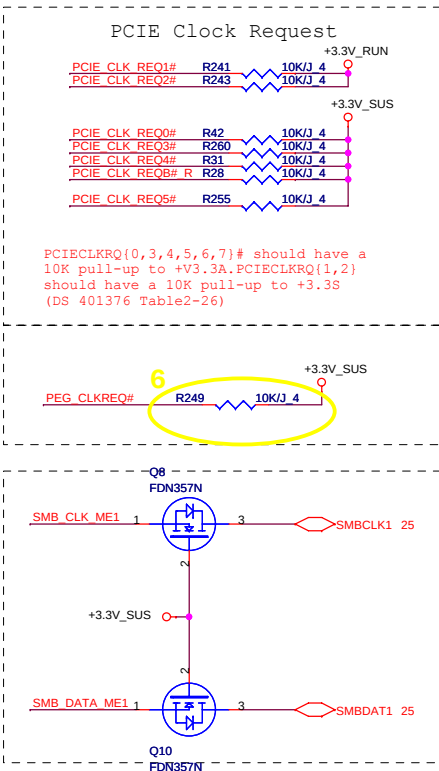


IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M (GND)

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB46	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC2	VSS[183]	VSS[283]	M5
BC22	VSS[184]	VSS[284]	M8
BC32	VSS[185]	VSS[285]	P11
BC36	VSS[186]	VSS[286]	AD15
BC40	VSS[187]	VSS[287]	P22
BC44	VSS[188]	VSS[288]	P30
BC52	VSS[189]	VSS[289]	P32
BH9	VSS[190]	VSS[290]	P34
BD48	VSS[191]	VSS[291]	P42
BD49	VSS[192]	VSS[292]	P45
BD5	VSS[193]	VSS[293]	P47
BE12	VSS[194]	VSS[294]	R2
BE16	VSS[195]	VSS[295]	R52
BE20	VSS[196]	VSS[296]	T12
BE24	VSS[197]	VSS[297]	T41
BE30	VSS[198]	VSS[298]	T46
BE34	VSS[199]	VSS[299]	T49
BE38	VSS[200]	VSS[300]	T5
BE42	VSS[201]	VSS[301]	T8
BE46	VSS[202]	VSS[302]	U30
BE48	VSS[203]	VSS[303]	U31
BE50	VSS[204]	VSS[304]	U32
BE6	VSS[205]	VSS[305]	U34
BE8	VSS[206]	VSS[306]	P38
BE9	VSS[207]	VSS[307]	V11
BEF3	VSS[208]	VSS[308]	V16
BEF9	VSS[209]	VSS[309]	V19
BG18	VSS[210]	VSS[310]	V20
BG24	VSS[211]	VSS[311]	V22
BG4	VSS[212]	VSS[312]	V30
BG50	VSS[213]	VSS[313]	V31
BH11	VSS[214]	VSS[314]	V32
BH15	VSS[215]	VSS[315]	V34
BH19	VSS[216]	VSS[316]	V35
BH23	VSS[217]	VSS[317]	V38
BH31	VSS[218]	VSS[318]	V43
BH35	VSS[219]	VSS[319]	V45
BH39	VSS[220]	VSS[320]	V46
BH43	VSS[221]	VSS[321]	V47
BH47	VSS[222]	VSS[322]	V49
BH7	VSS[223]	VSS[323]	V5
C12	VSS[224]	VSS[324]	V7
C50	VSS[225]	VSS[325]	V8
D51	VSS[226]	VSS[326]	W2
E12	VSS[227]	VSS[327]	W52
E16	VSS[228]	VSS[328]	Y11
E20	VSS[229]	VSS[329]	Y12
E24	VSS[230]	VSS[330]	Y15
E30	VSS[231]	VSS[331]	Y19
E34	VSS[232]	VSS[332]	Y23
E38	VSS[233]	VSS[333]	Y28
E42	VSS[234]	VSS[334]	Y30
E46	VSS[235]	VSS[335]	Y31
E48	VSS[236]	VSS[336]	Y32
E6	VSS[237]	VSS[337]	Y38
E8	VSS[238]	VSS[338]	Y43
F49	VSS[239]	VSS[339]	Y46
F5	VSS[240]	VSS[340]	P49
G10	VSS[241]	VSS[341]	Y5
G14	VSS[242]	VSS[342]	Y6
G18	VSS[243]	VSS[343]	Y8
G2	VSS[244]	VSS[344]	Y13
G22	VSS[245]	VSS[345]	AD51
G32	VSS[246]	VSS[346]	AT8
G36	VSS[247]	VSS[347]	AD47
G40	VSS[248]	VSS[348]	Y47
G44	VSS[249]	VSS[349]	AT12
G52	VSS[250]	VSS[350]	AM6
AF39	VSS[251]	VSS[351]	AT13
H16	VSS[252]	VSS[352]	AM5
H20	VSS[253]	VSS[353]	AK45
H30	VSS[254]	VSS[354]	AK39
H34	VSS[255]	VSS[355]	AV14
H38	VSS[256]	VSS[356]	
H42	VSS[257]	VSS[357]	
H49	VSS[258]	VSS[358]	



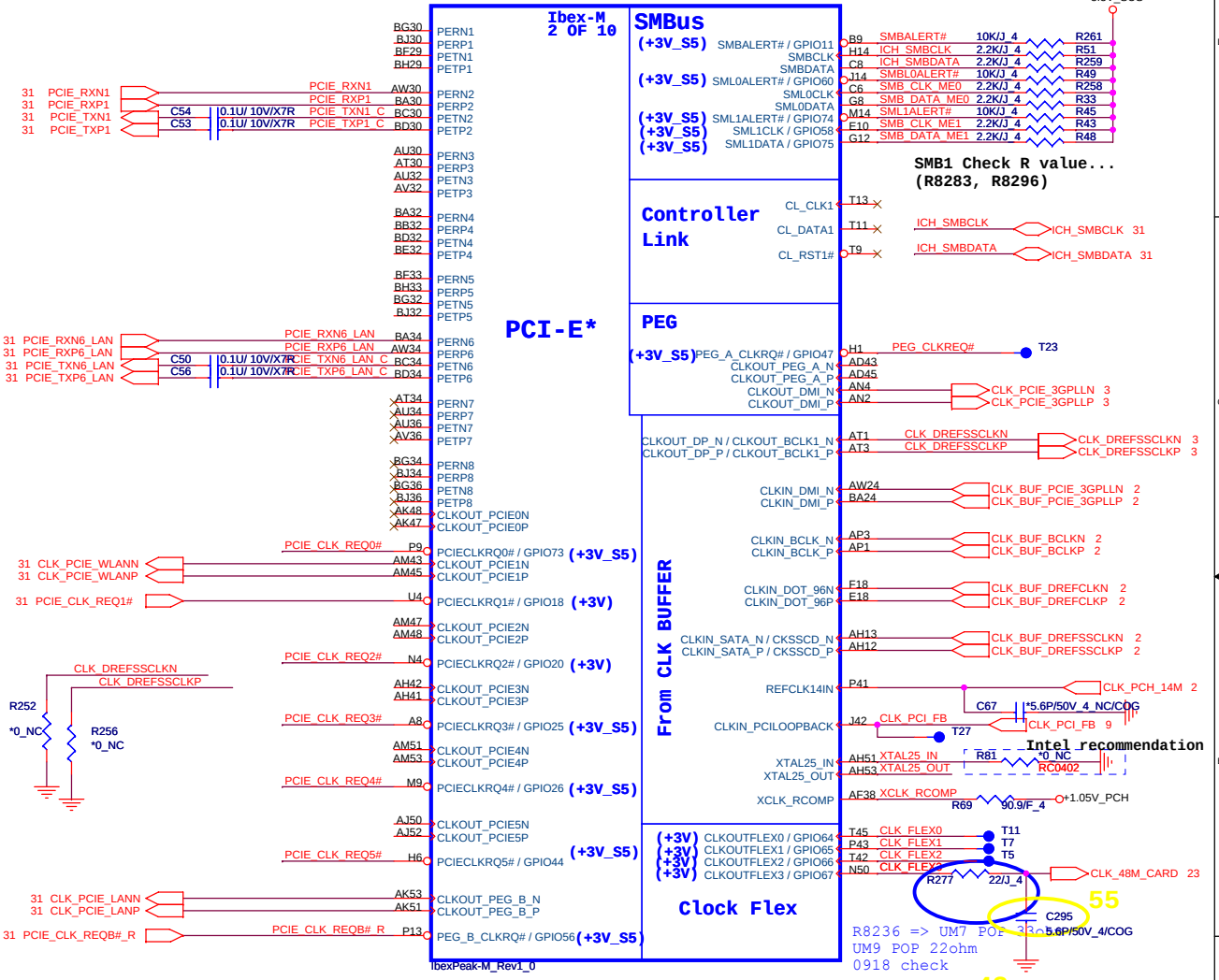
[WLAN]

[LAN]

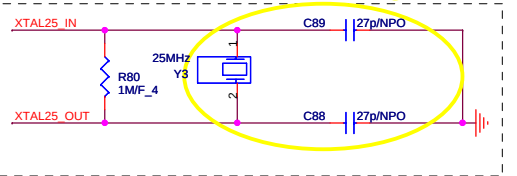
MiniWLAN

LAN

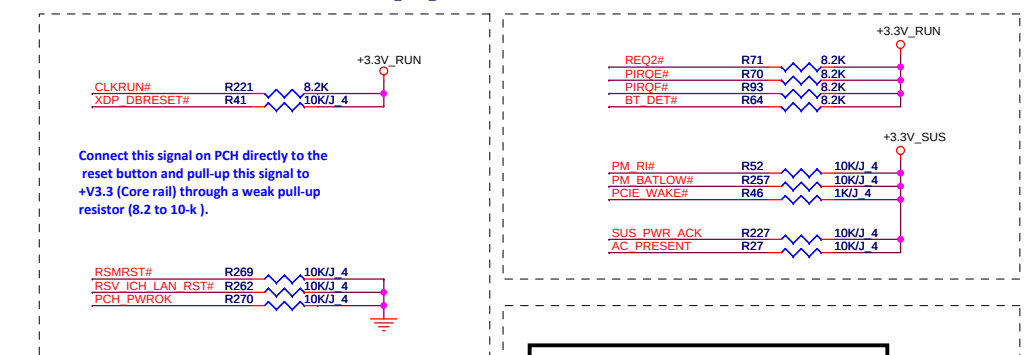
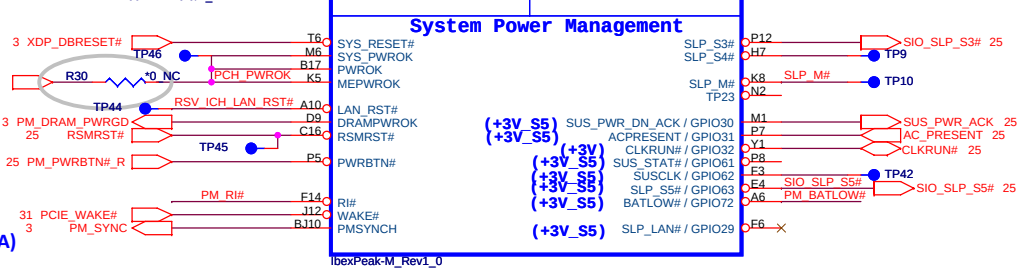
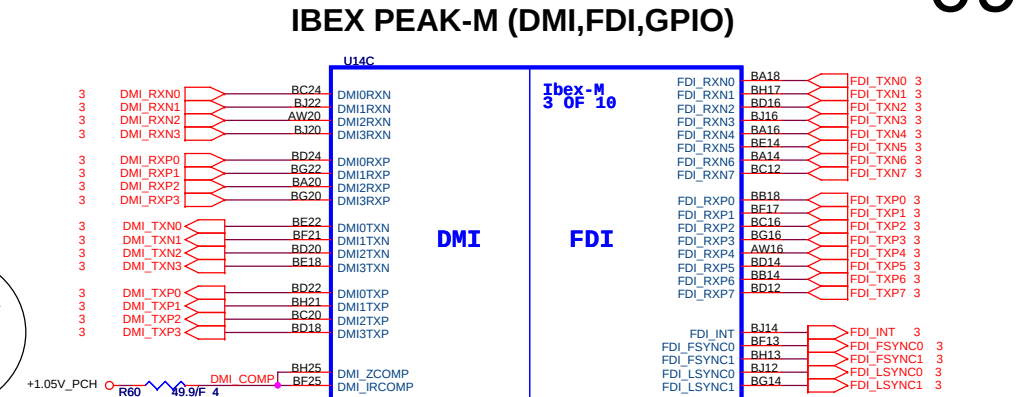
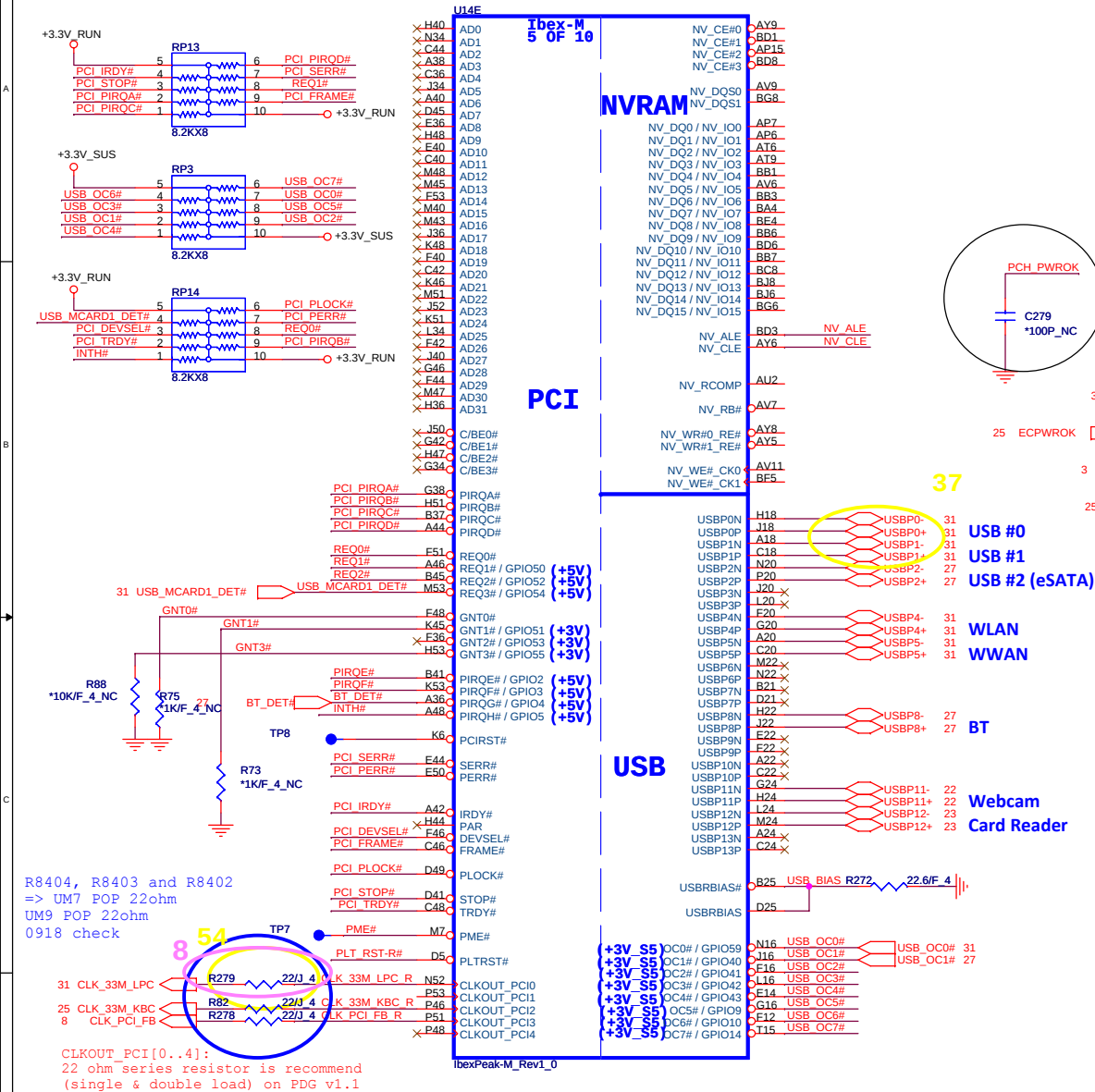
IBEX PEAK-M (PCI-E,SMBUS,CLK)



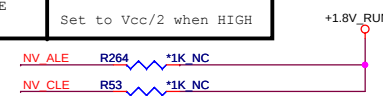
UMA	POP Y8201, C8411, C8412 and R8401, de-POP R8999 for Internal GFX
DIS	de-POP Y8201, C8411, C8412 and R8401, POP R8999 for Internal GFX



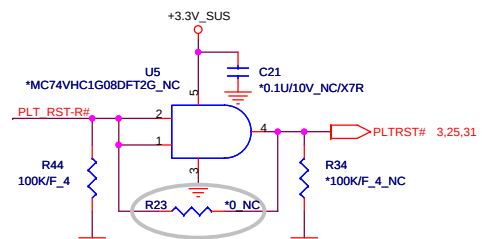
IBEX PEAK-M (PCI,USB,NVRAM)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

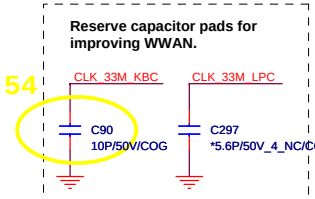


Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



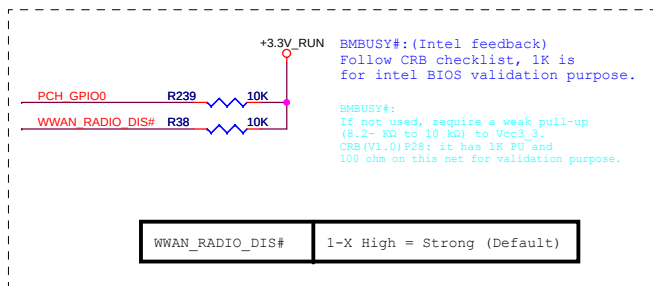
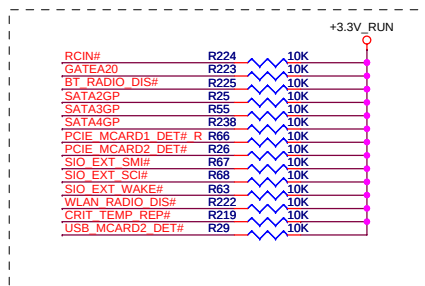
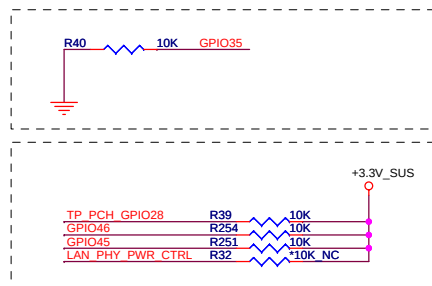
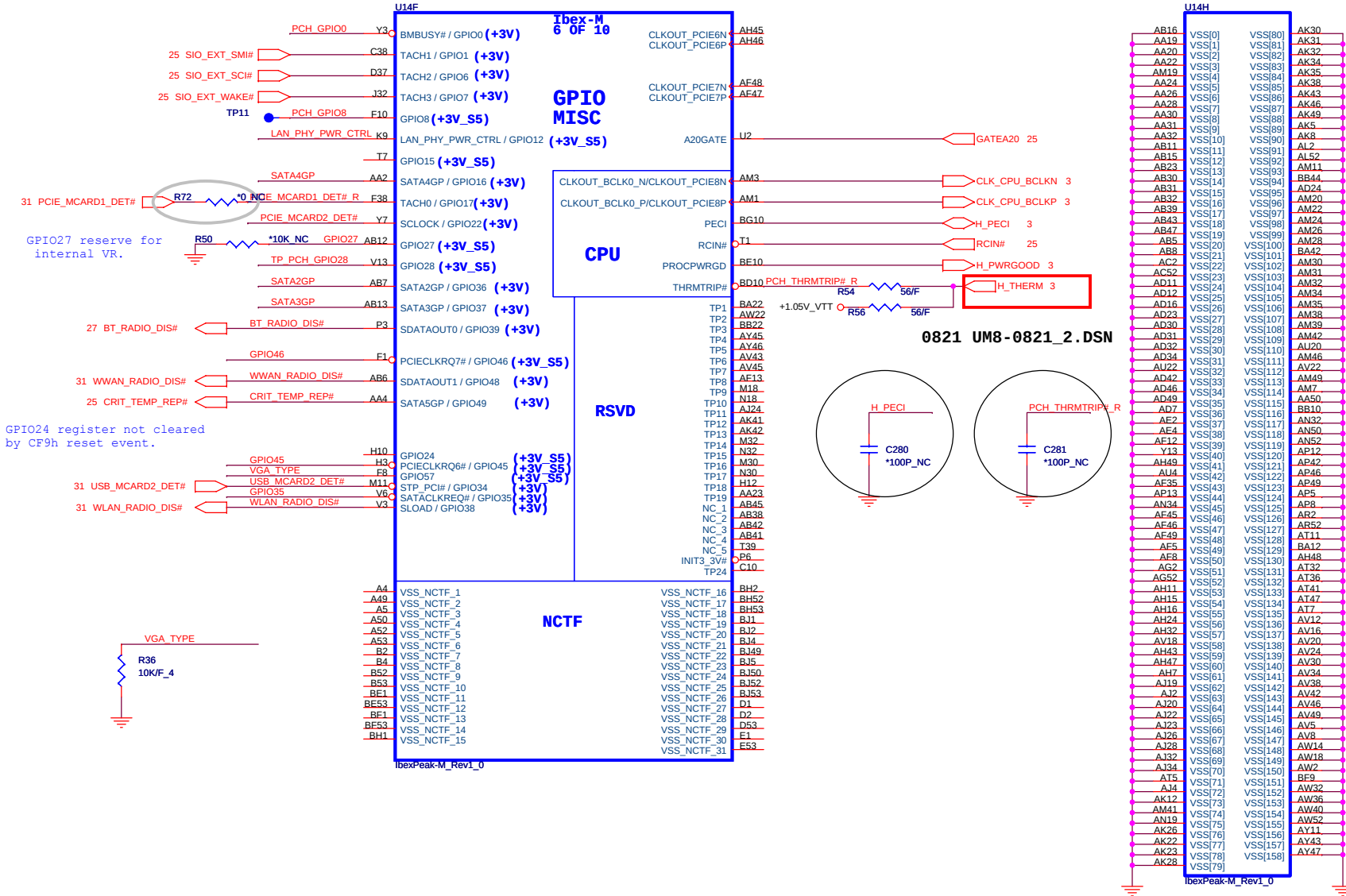
Boot BIOS Strap		
GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
CG	GNT3# Low = A16 swap override/Top-Block Swap Override enabled High = Default



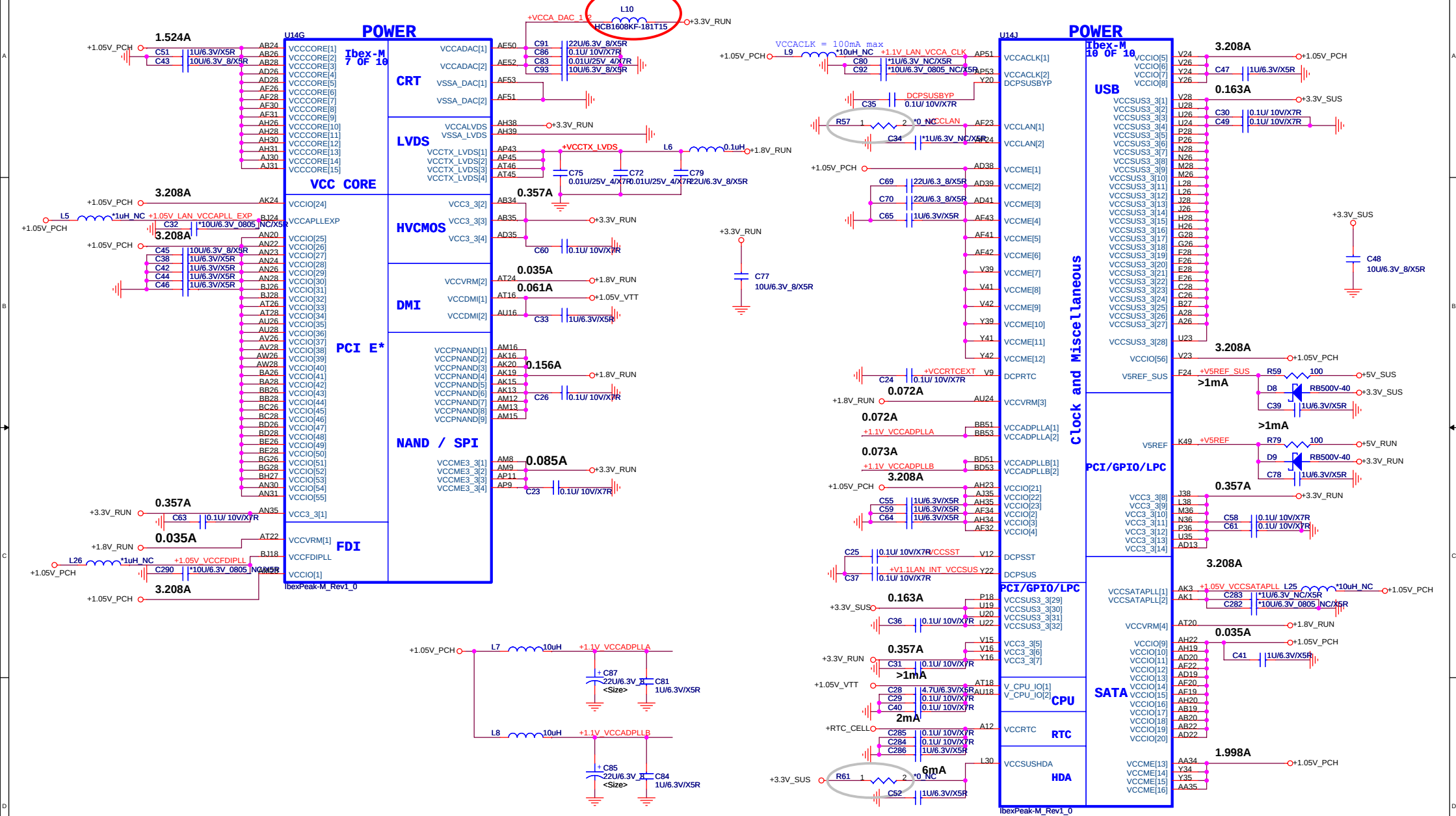
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

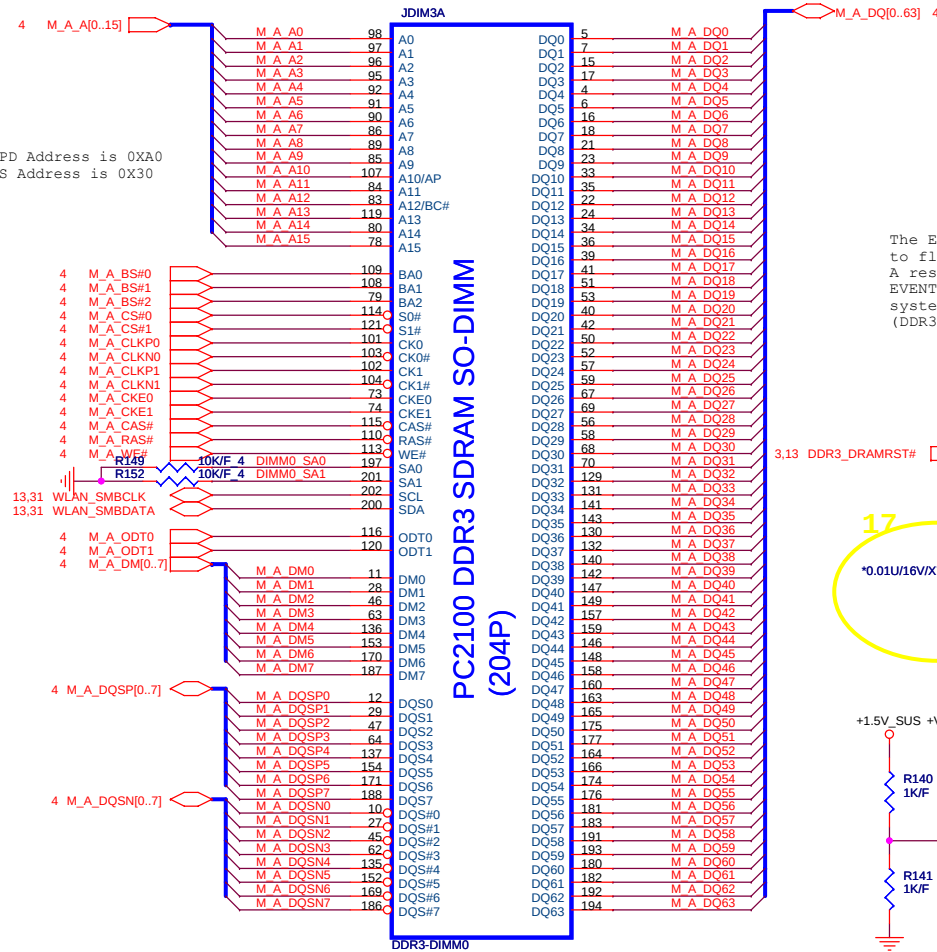


Cap quantities follow UM3

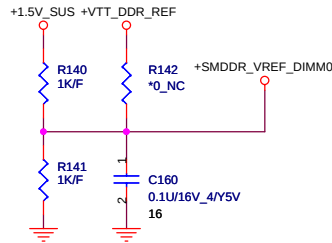
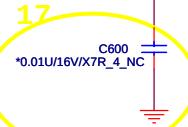
need check to change to 470 ohm



SO-DIMM SPD Address is 0XA0
SO-DIMM TS Address is 0X30



The EVENT# pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT# bus line to Vddspd on the system planer to act as a pullup. (DDR3 DS REV0.5)



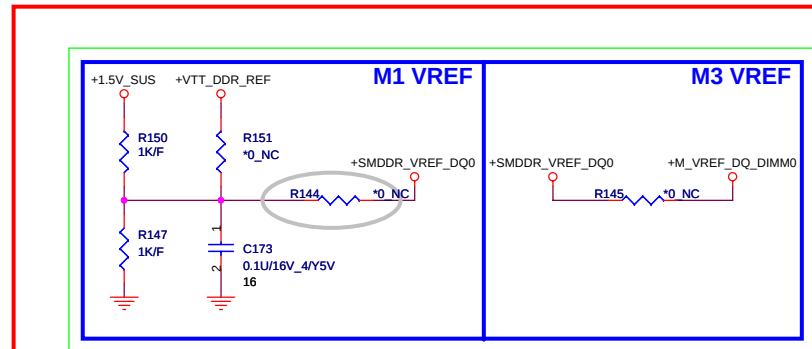
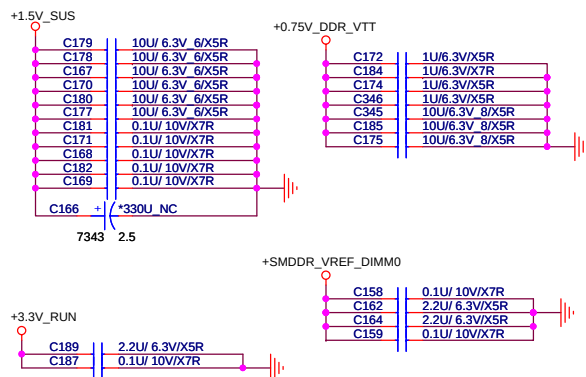
M2 VREF

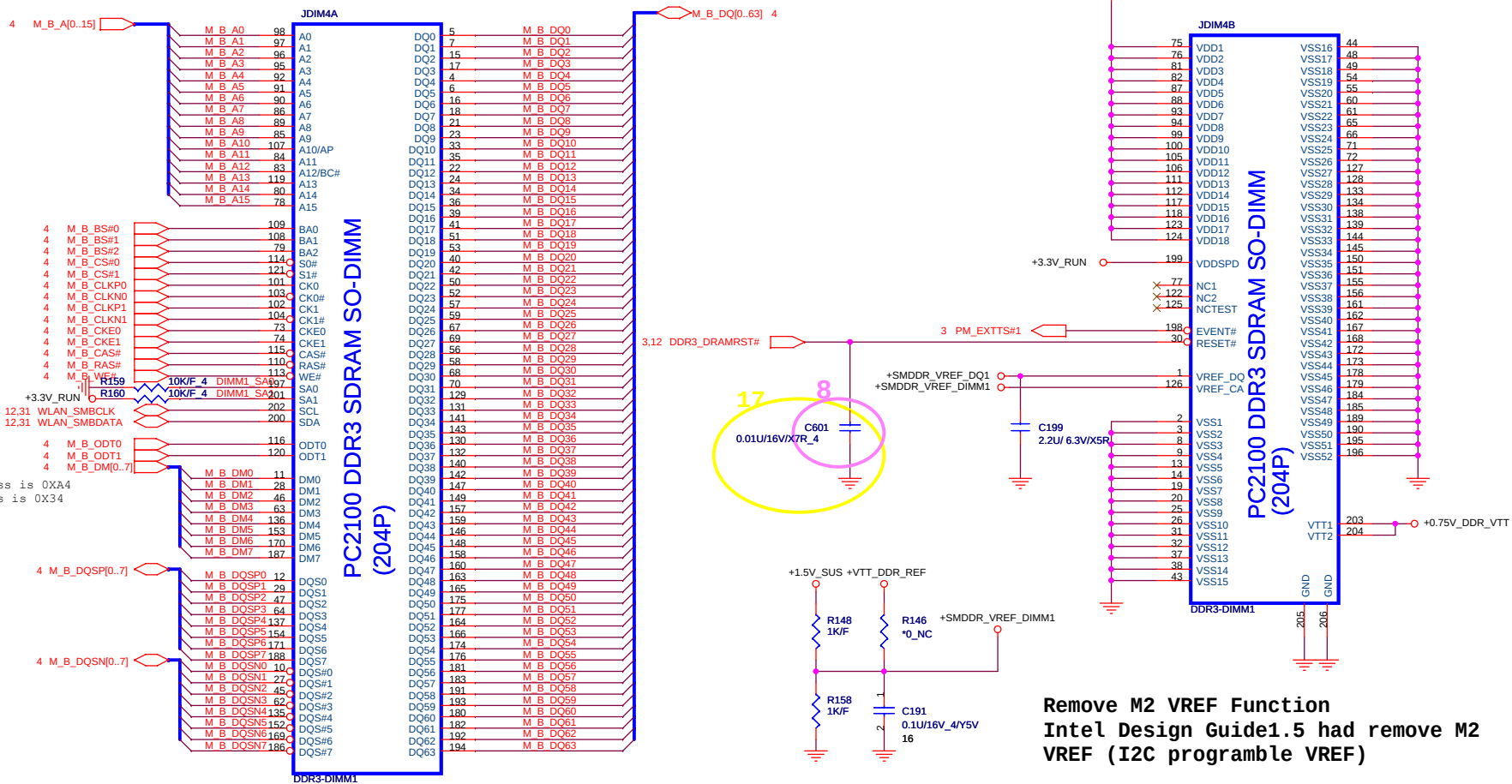
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



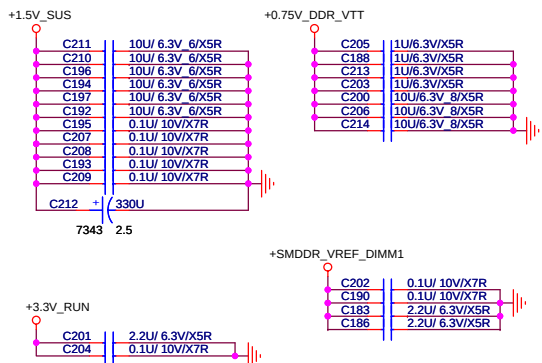


Remove M2 VREF Function
Intel Design Guide1.5 had remove M2
VREF (I2C programable VREF)

M3 => support for Clarksfield processor

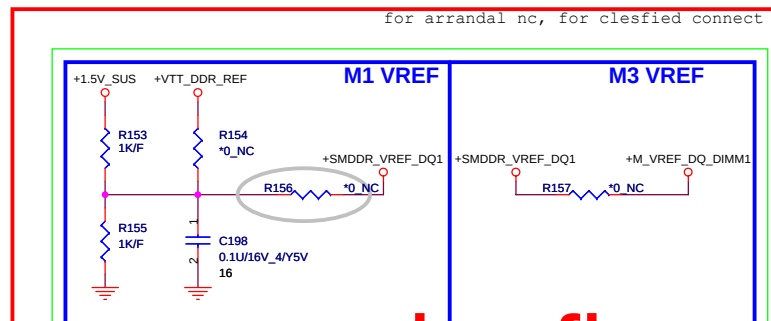
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Wait Victor check

for arrandal nc, for clesfied connect



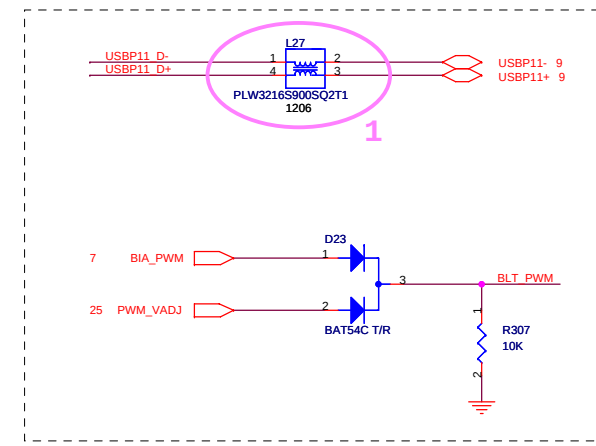
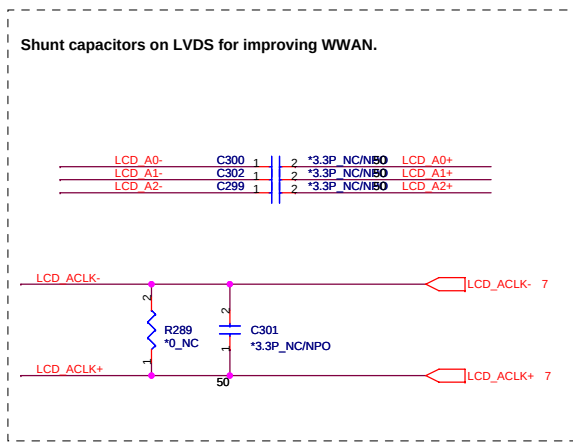
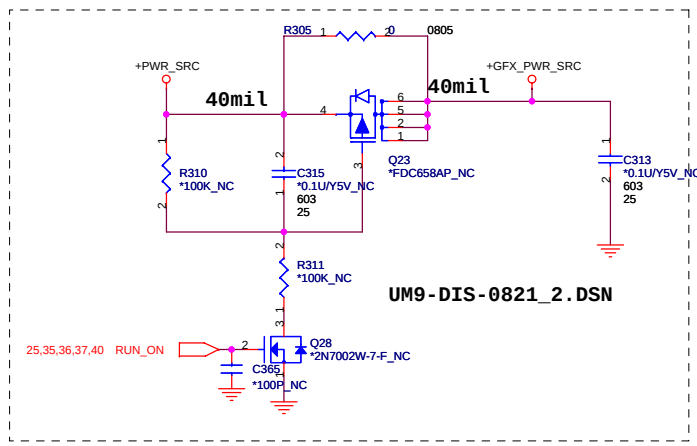
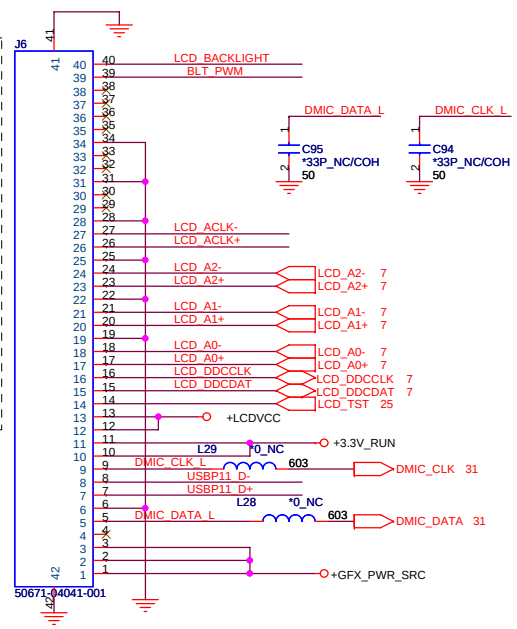
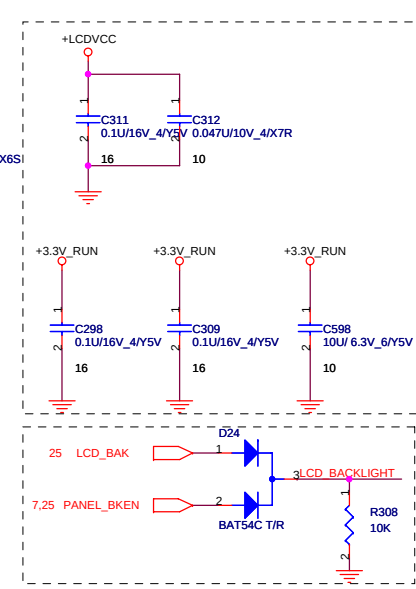
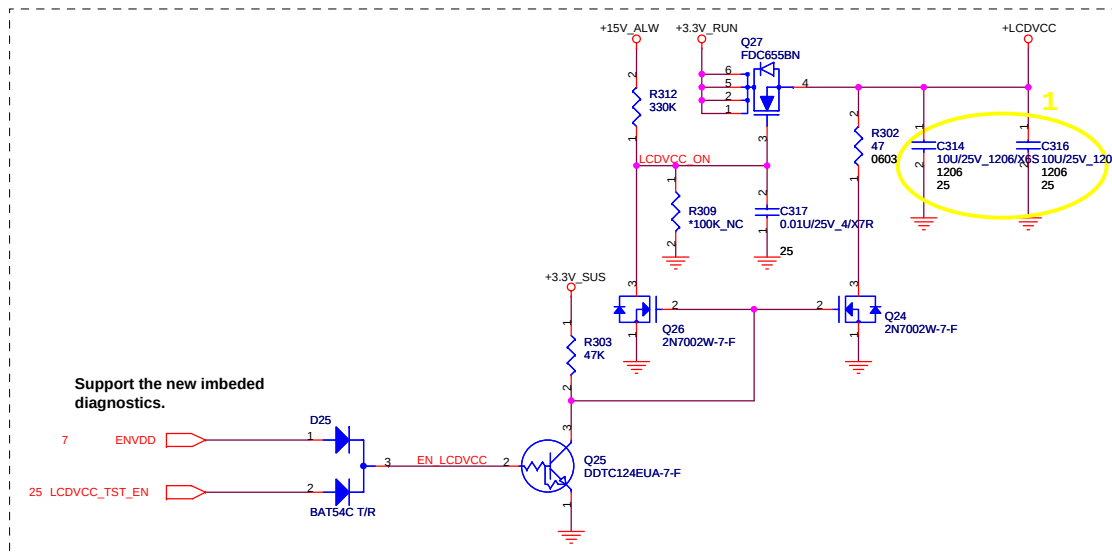


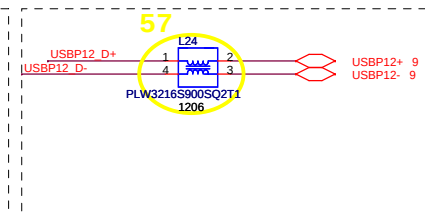
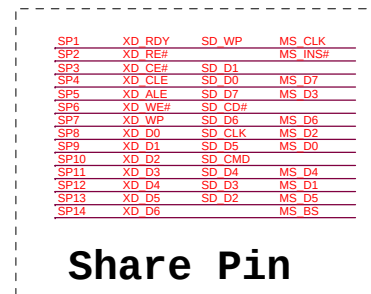
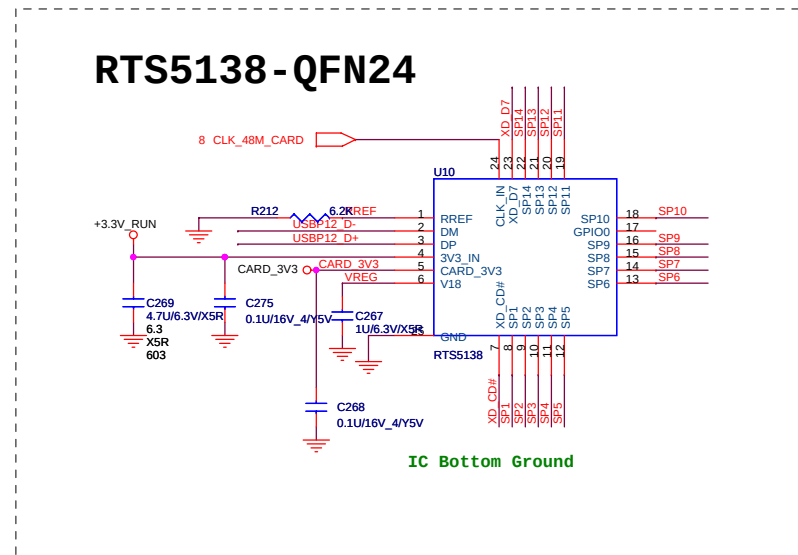
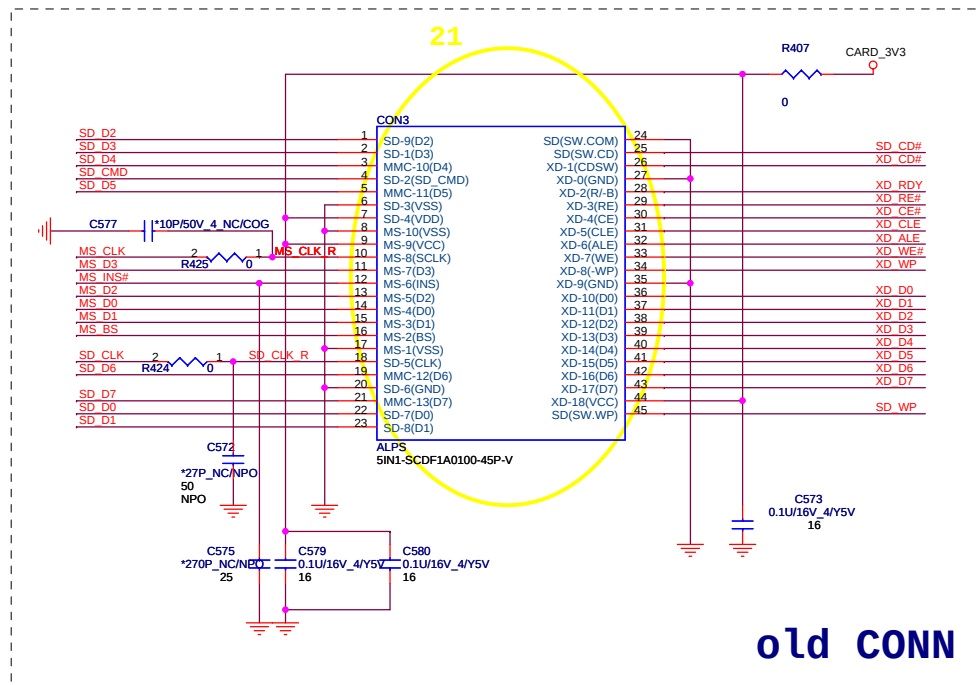
	5	4	3	2	1
D					
C					
B					
A					

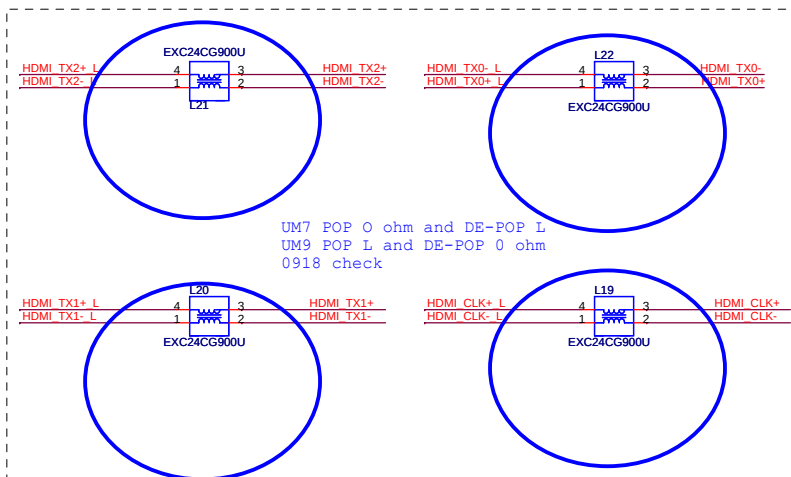




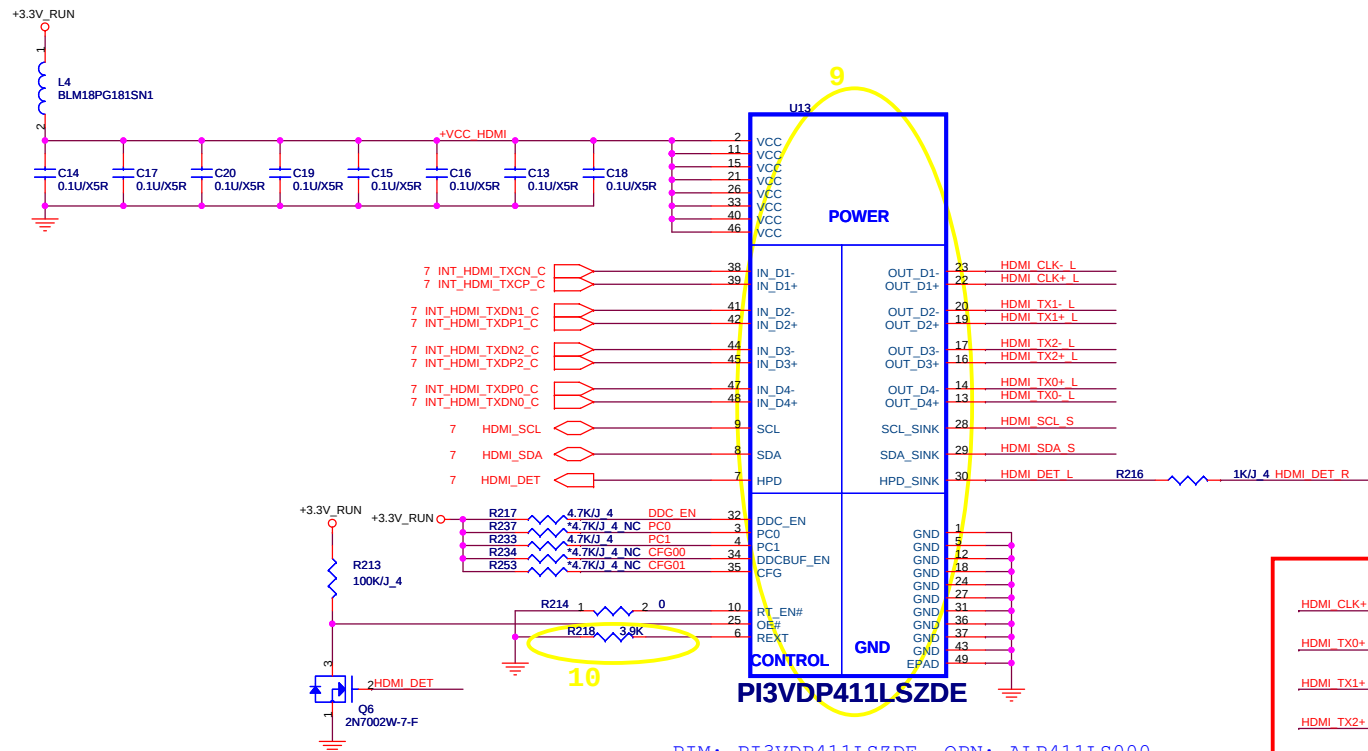
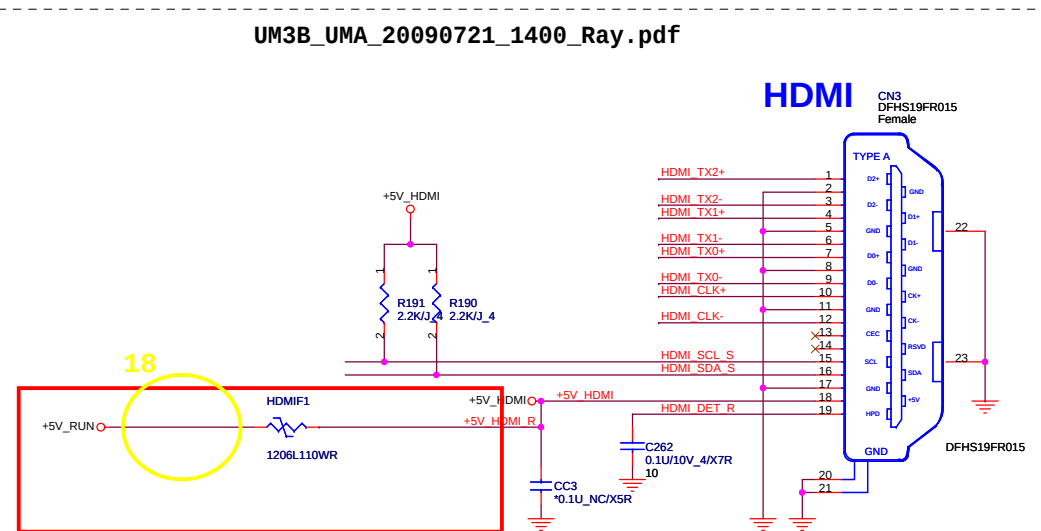








UM7 POP 0 ohm and DE-POP L
UM9 POP L and DE-POP 0 ohm
0918 check

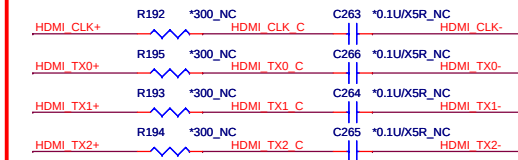
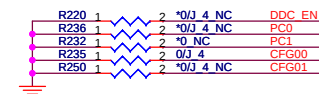


PIM: PI3VDP411LSZDE QPN: ALP411LS000
TI: SN75DP139RGZR QPN: AL000139000

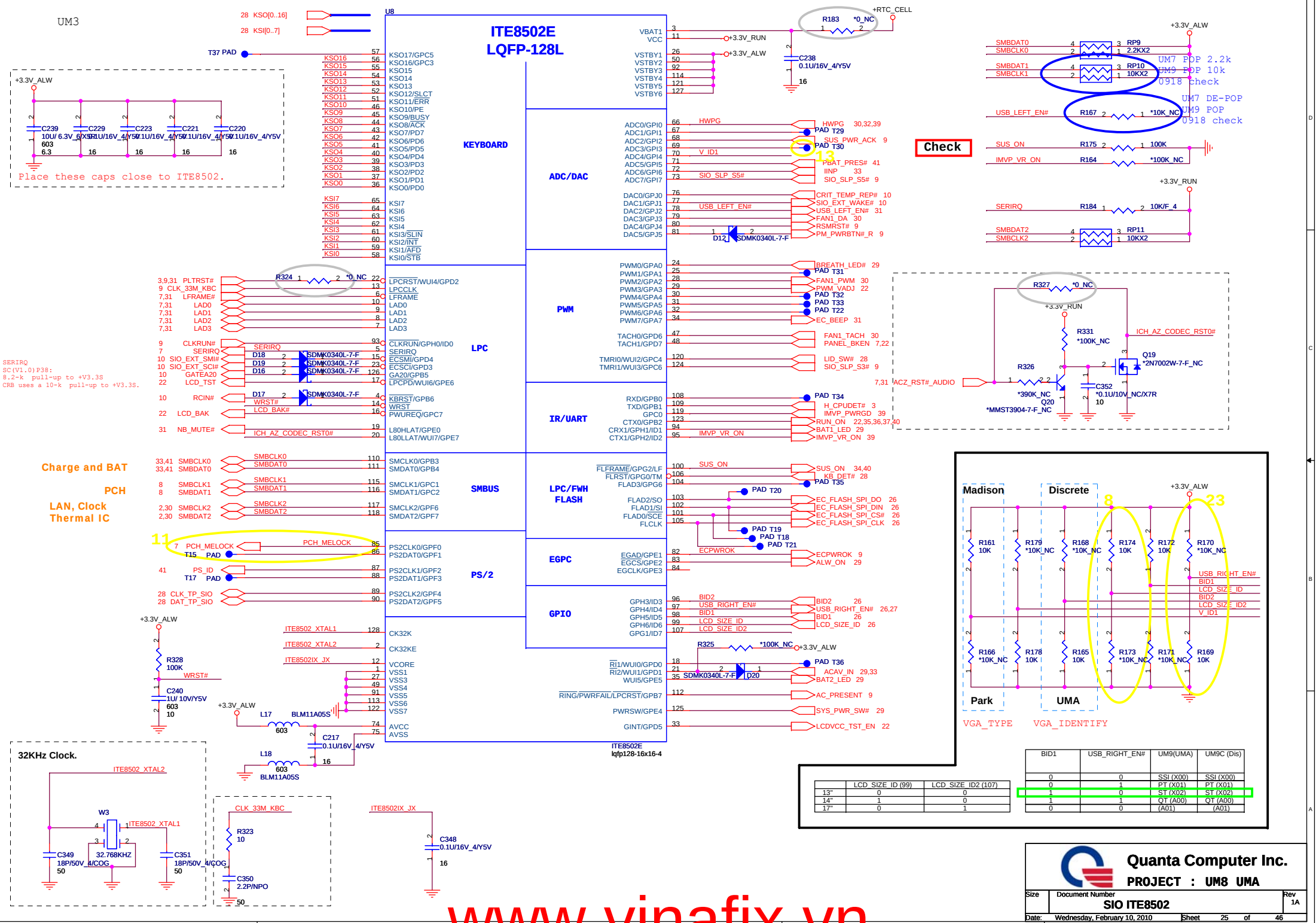
SCLZ/SDAZ Low-level input/output Voltage	
CFG01:CFG00=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1	VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0	VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1	VIL:<0.36V VOL:0.6V

EQUALIZATION SETTING	
PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommended
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

HDMI_PWR_CTRL
0 is Enable
1 is Disable



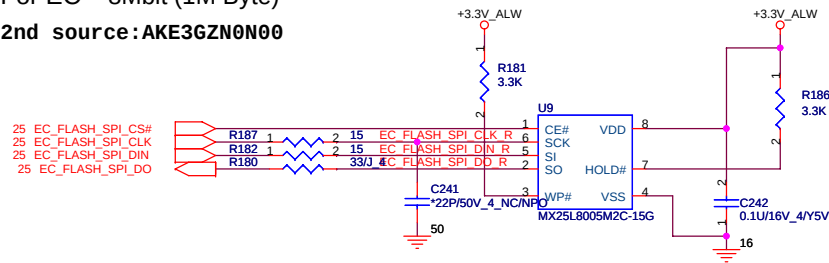
Reserve for EMI



UM3

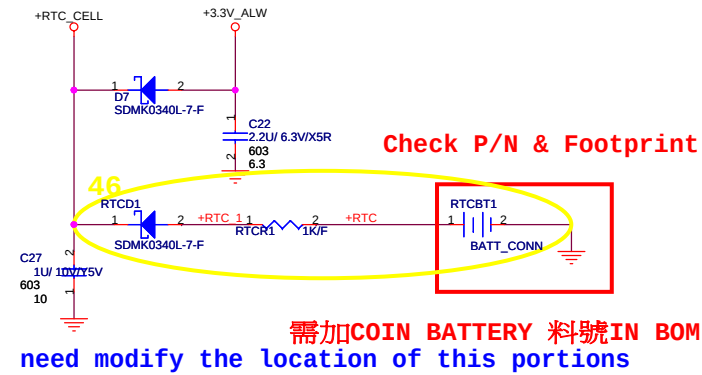
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

RTC BATTERY



Check P/N & Footprint

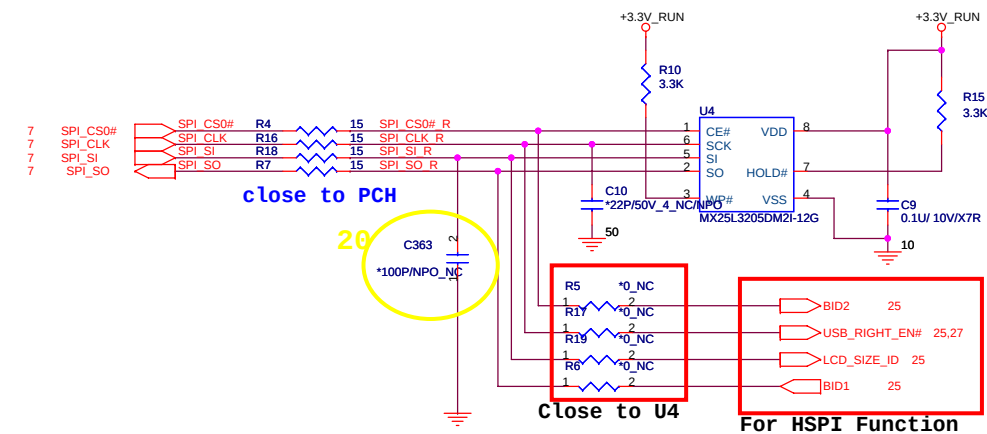
需加COIN BATTERY 料號IN BOM
need modify the location of this portions



For PCH

32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00



close to PCH

20

close to U4

For HSPI Function



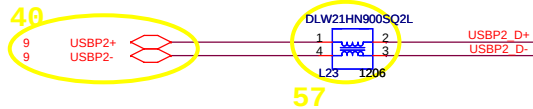
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	FLASH/RTC	1A
Date:	Wednesday, February 10, 2010	Sheet 26 of 46

www.vinafix.vn

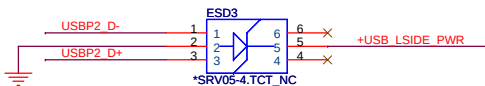
eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

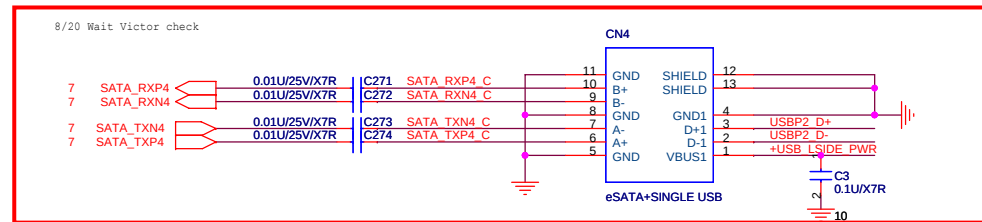


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

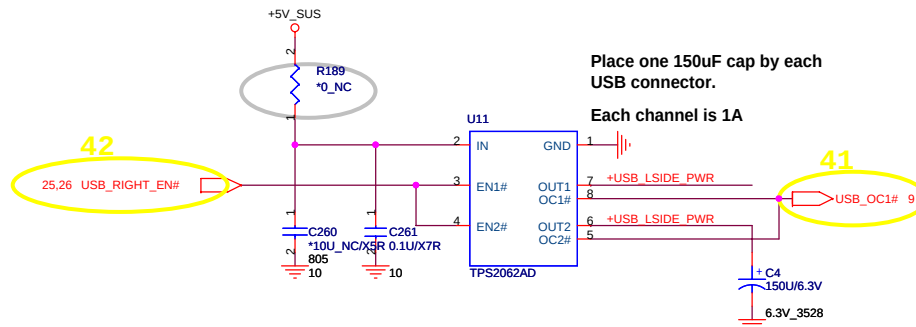


USB and eSATA Conn.



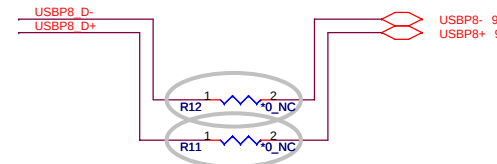
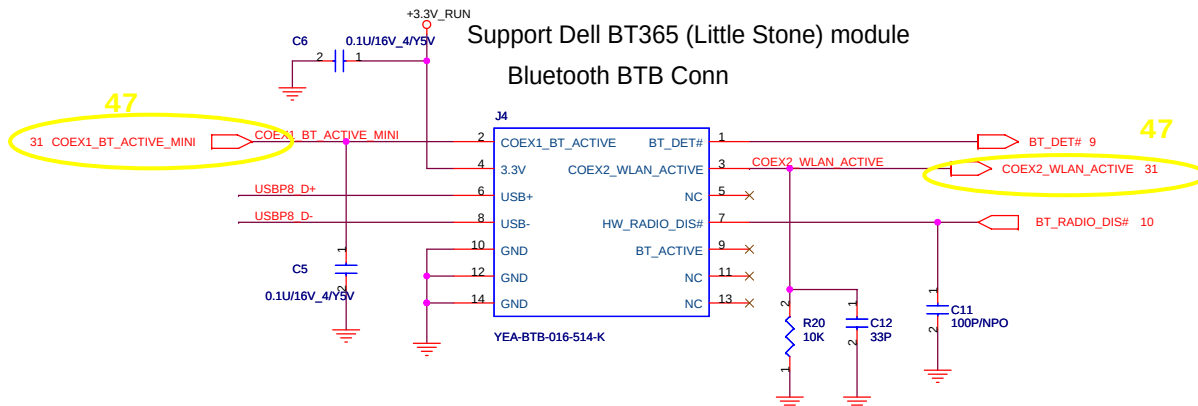
Place one 150uF cap by each USB connector.

Each channel is 1A



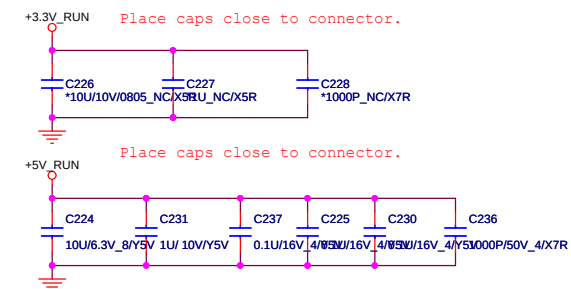
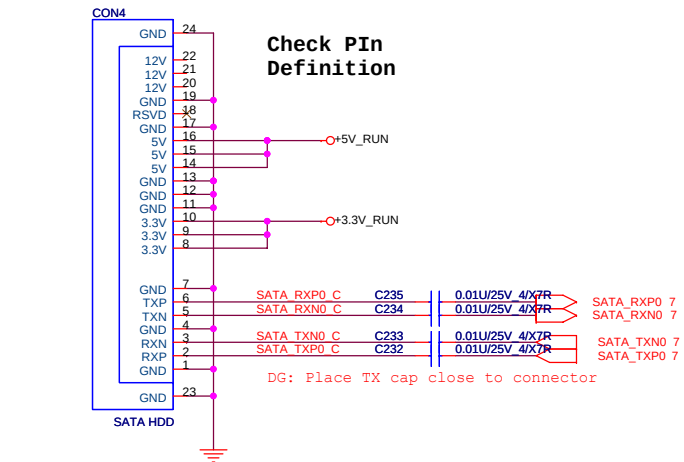
Support Dell BT365 (Little Stone) module

Bluetooth BTB Conn

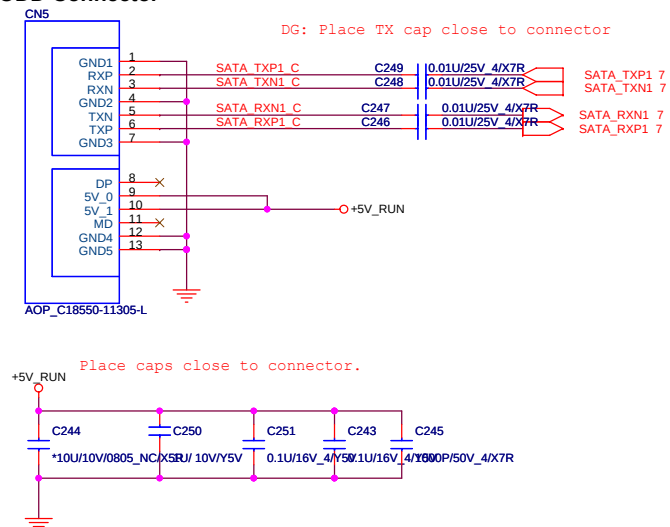


Quanta Computer Inc.
PROJECT : UM8 UMA

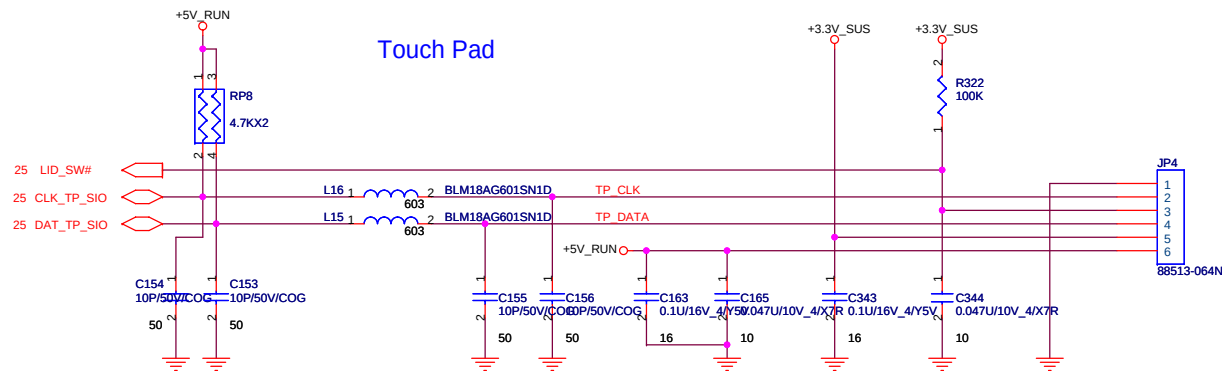
SATA Connector.



ODD Connector

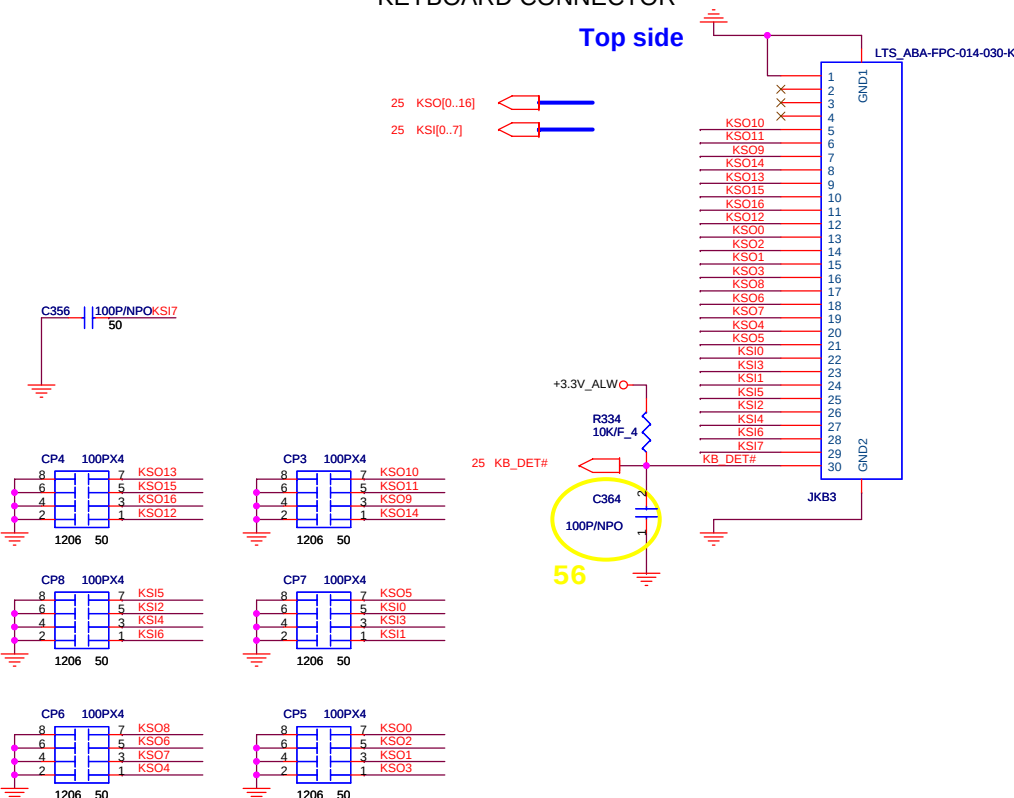


Touch Pad



KEYBOARD CONNECTOR

Top side



100P CAPS CLOSE TO JKB1



Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	SATA (HDD&ODD) & TP & KB	1A
Date:	Wednesday, February 10, 2010	Sheet 28 of 46

Power

High output current driver 24mA

check output current for 3 LED

31 BREATH_PWRLED

BREATH_PWRLED

R8 390

D3 HT-S91BP5

15

WHITE

2N7002W-7-F

U3 TC7SZ04FU(T5L,F,T)

100K

25 BREATH_LED#

BREATH_PWRLED

3.3V_SUS

5V_SUS

5V_SUS

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

126

127

128

129

130

131

132

133

134

135

136

137

138

139

140

141

142

143

144

145

146

147

148

149

150

151

152

153

154

155

156

157

158

159

160

161

162

163

164

165

166

167

168

169

170

171

172

173

174

175

176

177

178

179

180

181

182

183

184

185

186

187

188

189

190

191

192

193

194

195

196

197

198

199

200

201

202

203

204

205

206

207

208

209

210

211

212

213

214

215

216

217

218

219

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235

236

237

238

239

240

241

242

243

244

245

246

247

248

249

250

251

252

253

254

255

256

257

258

259

260

261

262

263

264

265

266

267

268

269

270

271

272

273

274

275

276

277

278

279

280

281

282

283

284

285

286

287

288

289

290

291

292

293

294

295

296

297

298

299

300

301

302

303

304

305

306

307

308

309

310

311

312

313

314

315

316

317

318

319

320

321

322

323

324

325

326

327

328

329

330

331

332

333

334

335

336

337

338

339

340

341

342

343

344

345

346

347

348

349

350

351

352

353

354

355

356

357

358

359

360

361

362

363

364

365

366

367

368

369

370

371

372

373

374

375

376

377

378

379

380

381

382

383

384

385

386

387

388

389

390

391

392

393

394

395

396

397

398

399

400

401

402

403

404

405

406

407

408

409

410

411

412

413

414

415

416

417

418

419

420

421

422

423

424

425

426

427

428

429

430

431

432

433

434

435

436

437

438

439

440

441

442

443

444

445

446

447

448

449

450

451

452

453

454

455

456

457

458

459

460

461

462

463

464

465

466

467

468

469

HDD activity LED.

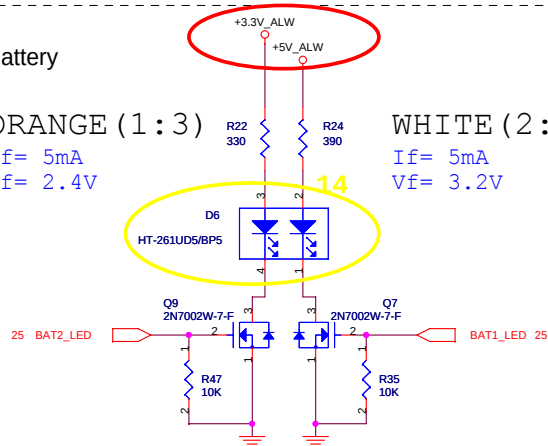
The diagram shows a circuit for an HDD activity LED. A +5V_RUN supply is connected to a 390 ohm resistor (R21) and the anode of a white LED (D5, HT-S91BP5). The cathode of the LED is connected to a 100K resistor (R9) and the emitter of a 2N7002W-7-F MOSFET (Q4). The gate of the MOSFET is connected to a SATA_LED# signal (pin 2) through a 2N7002W-7-F MOSFET (Q5). The drain of the MOSFET (Q4) is connected to the +5V_RUN supply. The MOSFET (Q5) is also connected to the +5V_RUN supply and ground.

ORANGE (1:3) R22 330 R24 390 WHITE (2:4)

If = 5mA If = 5mA

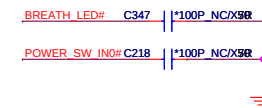
Vf = 2.4V Vf = 3.2V

14

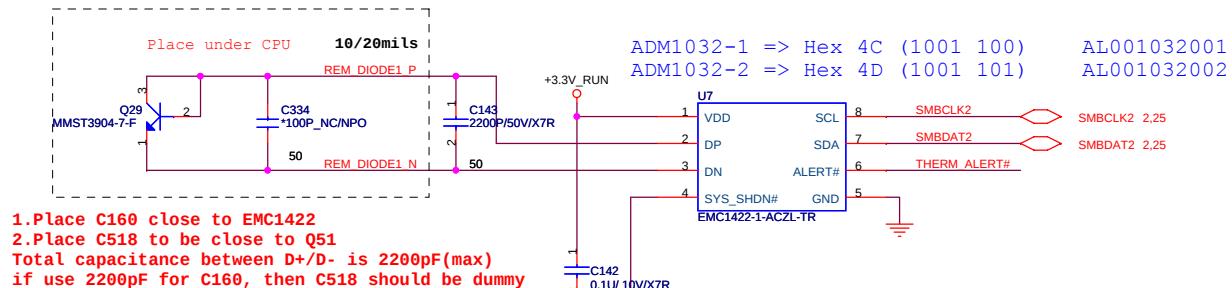
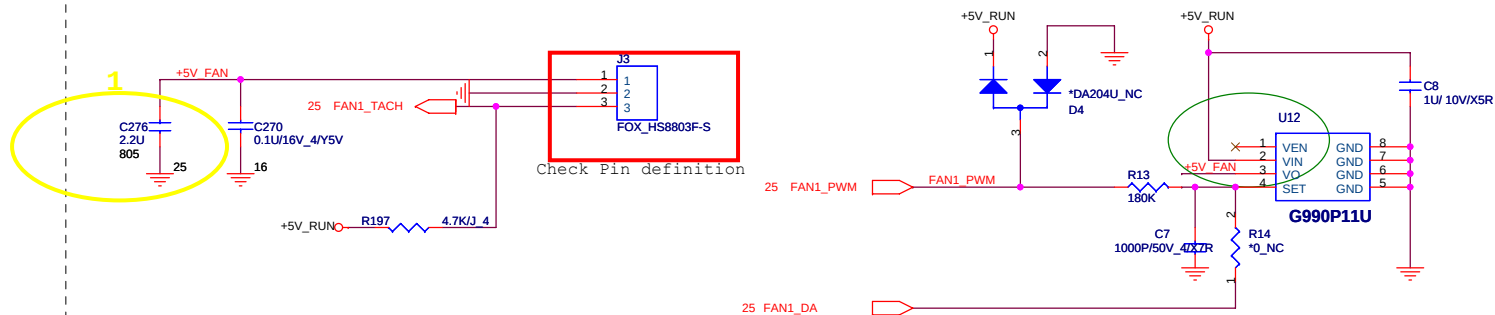


3VALW ON POWER LOGIC

The diagram illustrates the 3VALW ON POWER LOGIC circuit. It features a 3.3V_ALW input connected to a network of resistors (R163, R176, R162, R177) and diodes (D13, D14). The circuit also includes capacitors C215 and C216, and MOSFETs Q16, Q17, and Q18. The output is 3.3V_ALW_ON. A legend at the bottom specifies component values: BREATH_LED# C347 *100P_NC/X98 and POWER_SW_IN0# C218 *100P_NC/X98.



FAN CONTROL



1. Place C160 close to EMC1422
 2. Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

UM7 change this pin to H_VTTPWRGD

Follow UM3 to change Q11
PIN2 gate control to avoid
abnormal shutdown?

OTP 85 degree C

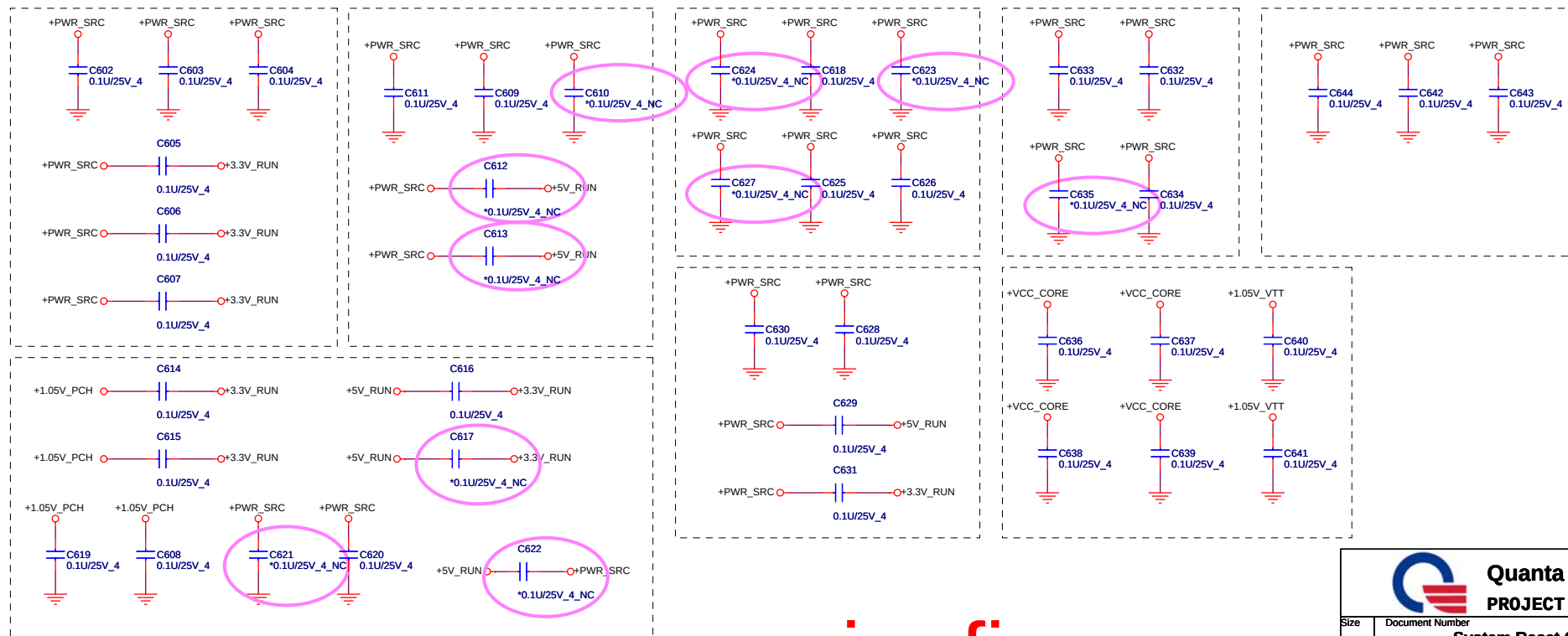
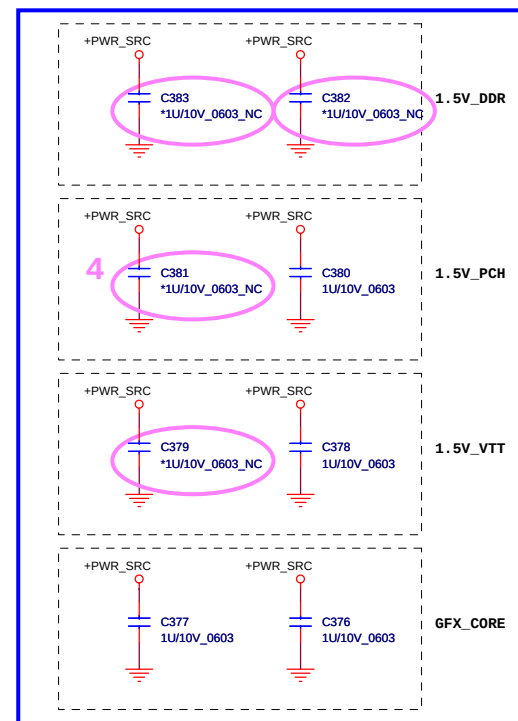
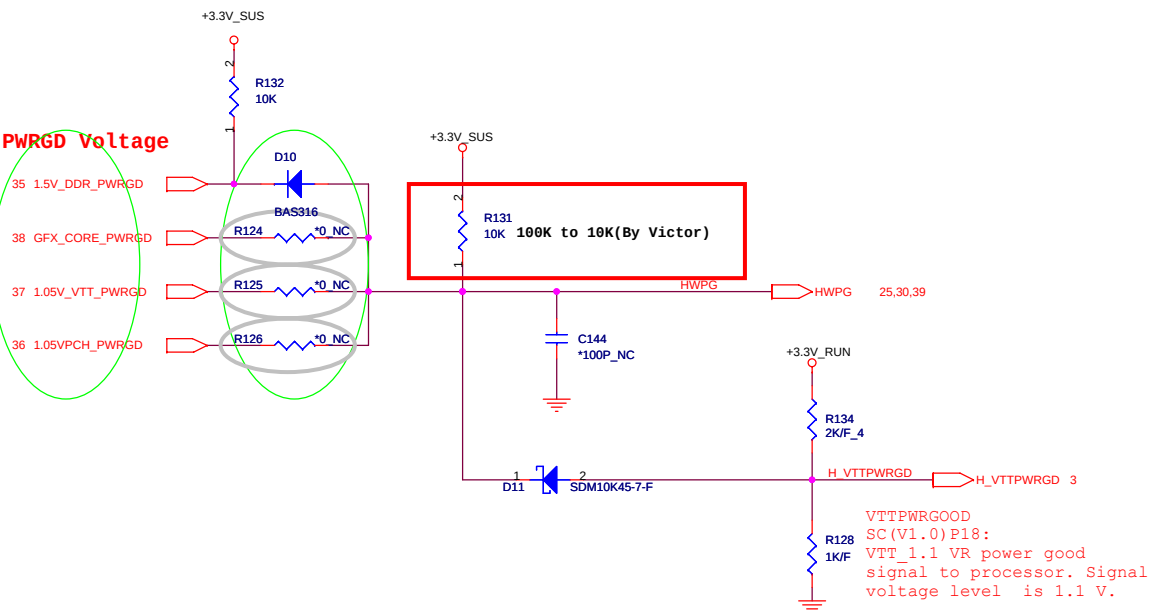


SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#						
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



Quanta Computer Inc.
PROJECT : UM8 UMA

Check PWRGD Voltage



www.vinafix.vn



Quanta Computer Inc.
PROJECT : UM8 UMA

+5V_SUS
Fs=200K
TDC : 7.8A
OCP : 11.1A

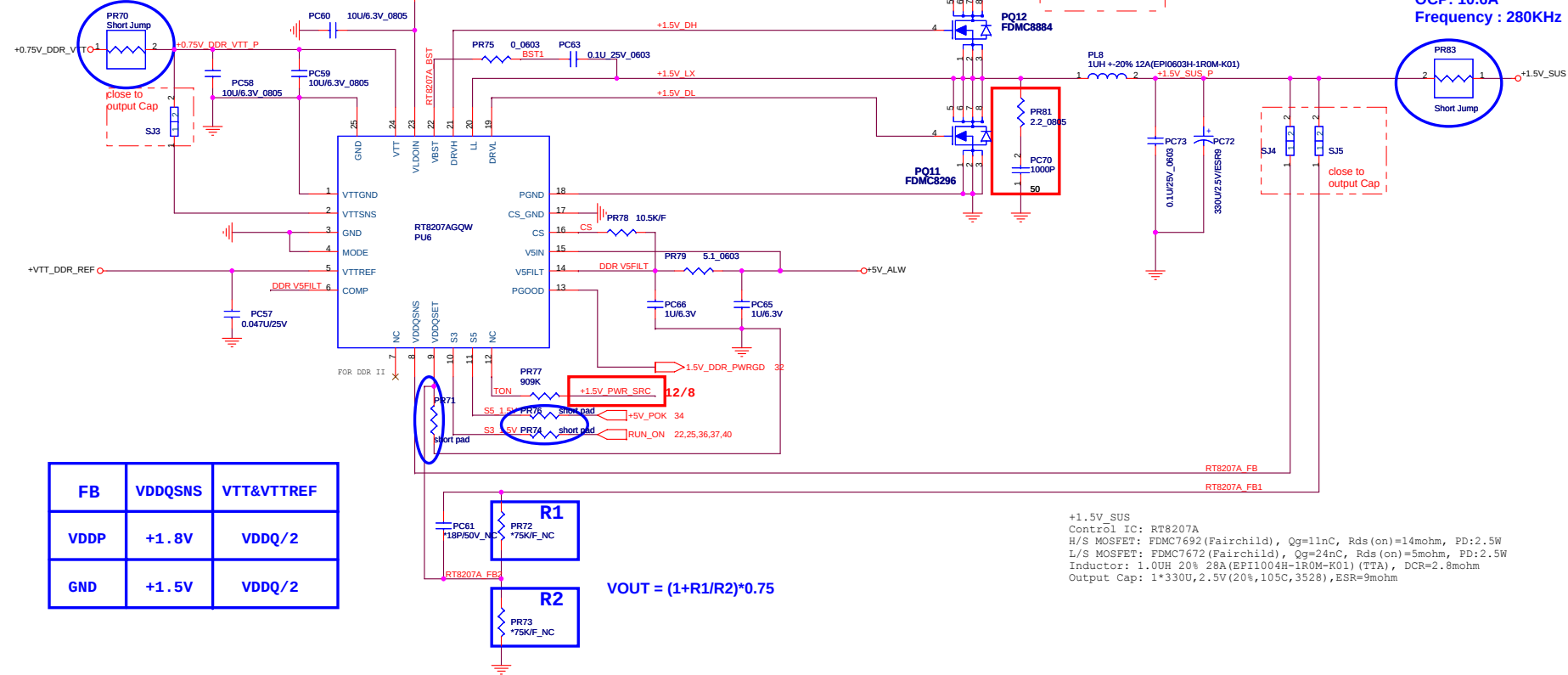
+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17,7343)

+3.3V_ALW
Fs=250K
TDC : 6.38(UMA) ; 7.6A(DIS)
OCP : 9.11(UMA) ; 10.9A(DIS)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17,7343)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

+0.75V_DDR_VTT
TDC : 0.7A

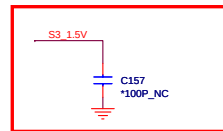


+1.5V_SUS
TDC : 7.4A
OCP: 10.6A
Frequency : 280KHz

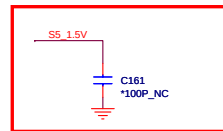
FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

$$VOUT = (1+R1/R2)*0.75$$

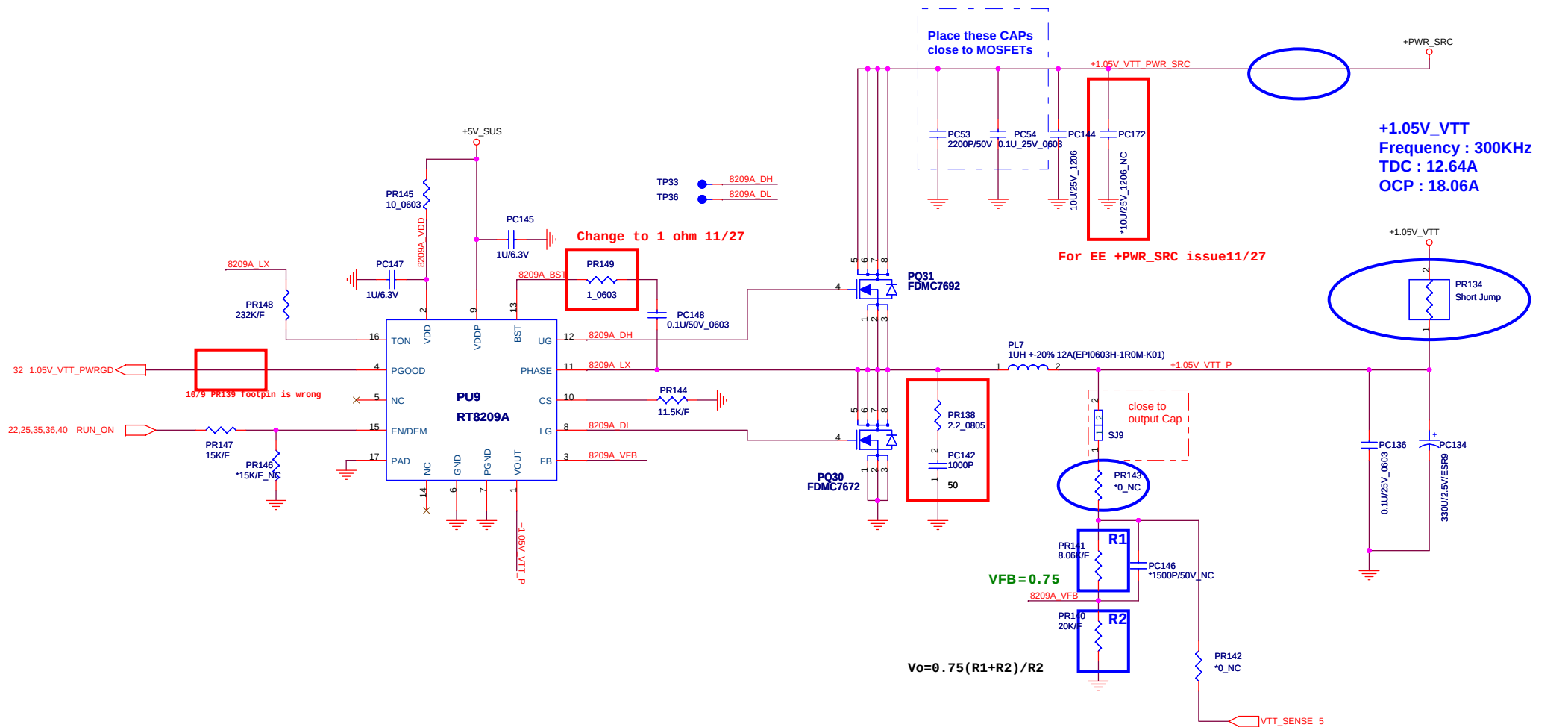
+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD=2.5W
L/S MOSFET: FDMC7672 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD=2.5W
Inductor: 1.0UH 20% 28A (EPI1004H-1ROM-K01) (TTA), DCR=2.8mohm
Output Cap: 1*330U, 2.5V (20%, 105C, 3528), ESR=9mohm



close to PR56



close to PR55

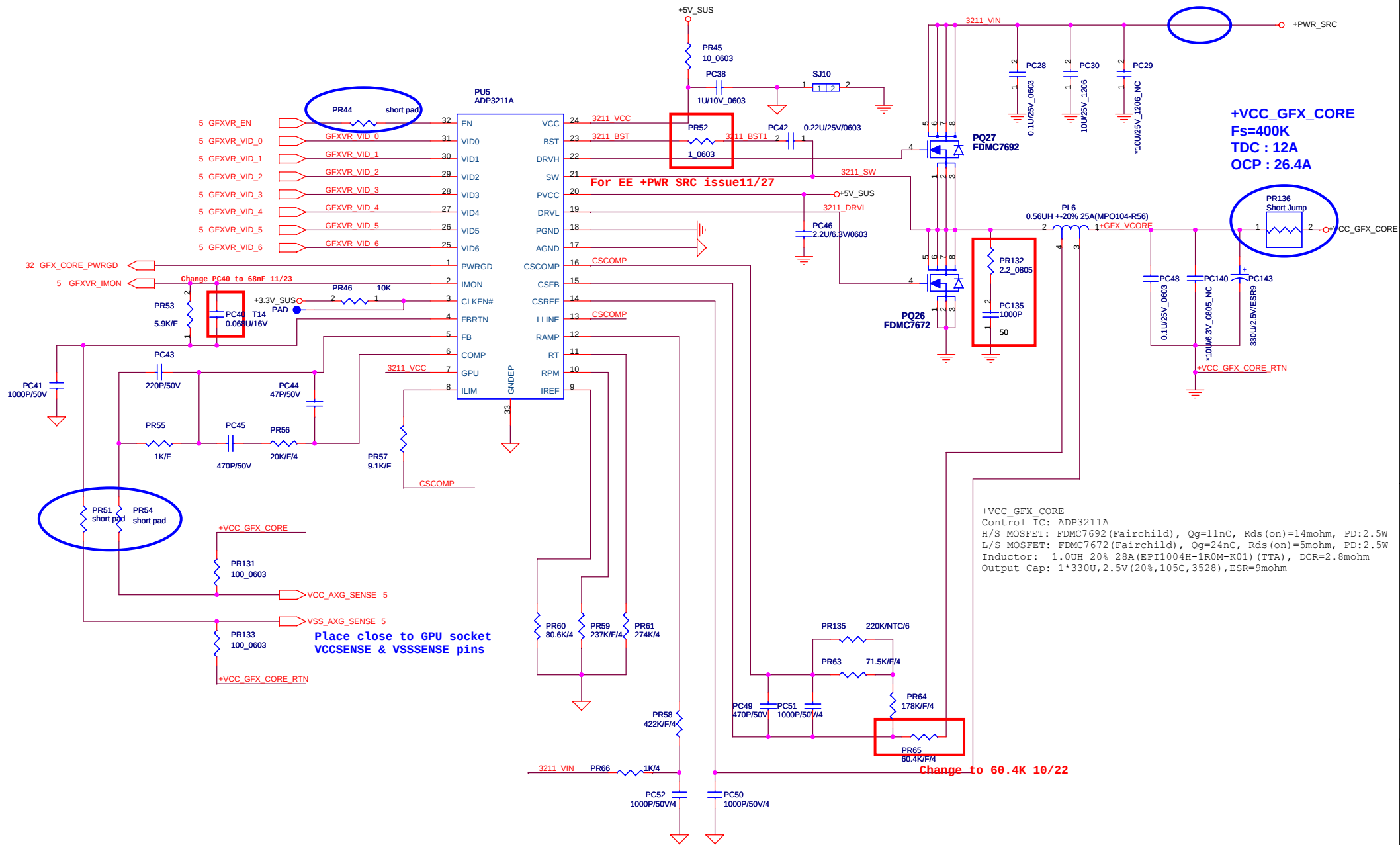


+1.05V VTT
Control IC: RT8209A
H/S MOSFET: FDMC7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A (EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
Output Cap: 1*330U, 2.5V (20%, 105C, 3528), ESR=9mohm



Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	1.05_VTT	1A
Date:	Wednesday, February 10, 2010	Sheet 37 of 44



Change to RUN_ON

22,25,35,36,37 RUN_ON

+5V_RUN
TDC : 5A

+3.3V_SUS
TDC : 0.26A

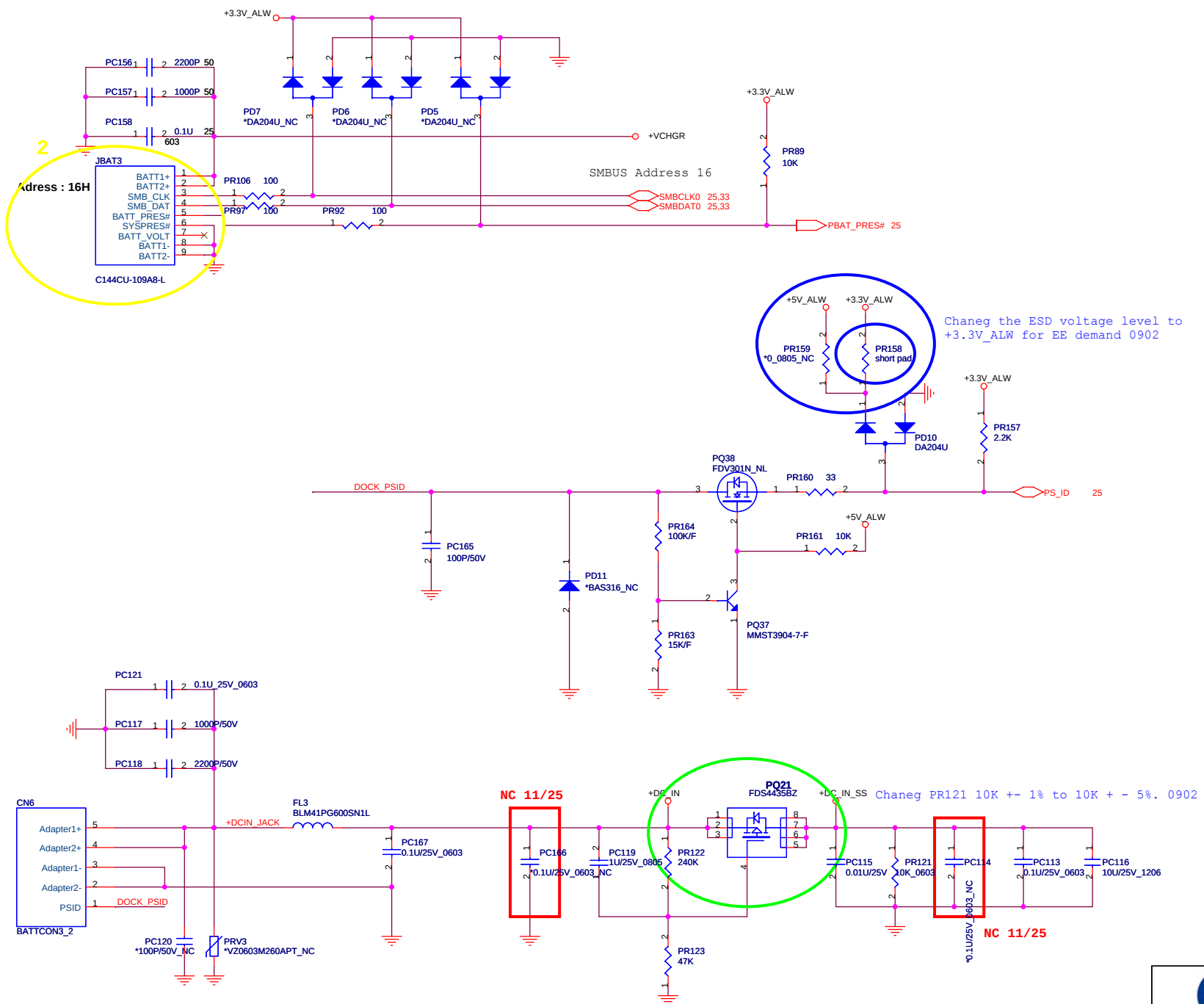
12/31 change to 0.01u for
Touch PAD issue - August

Change MOS spec 11/13

+1.5V_RUN
TDC : 0.35A

+3.3V_RUN
TDC : 4.9A

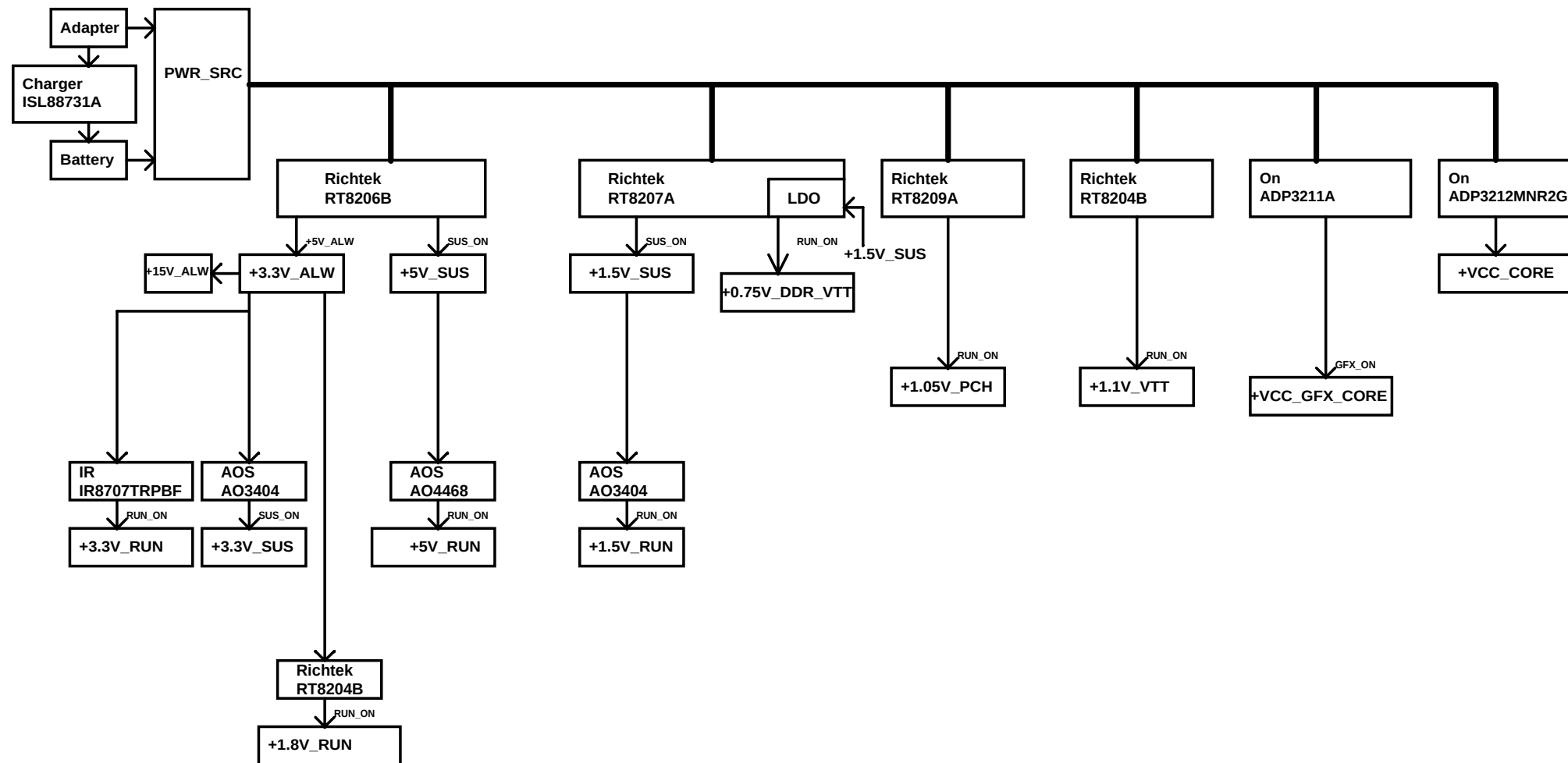
12/31 change to 0.01u for
Touch PAD issue - August

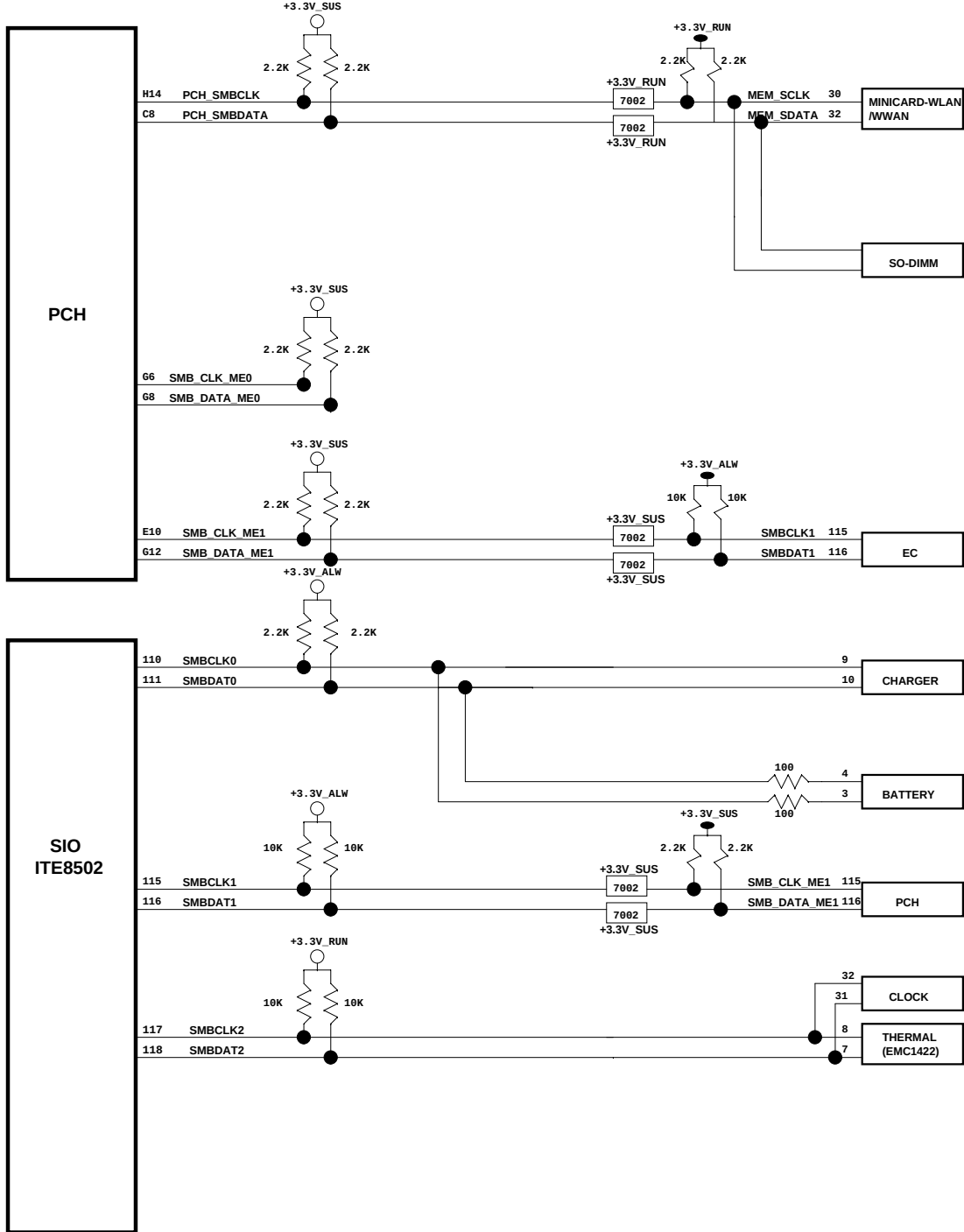


Quanta Computer Inc.
PROJECT : UM8 UMA

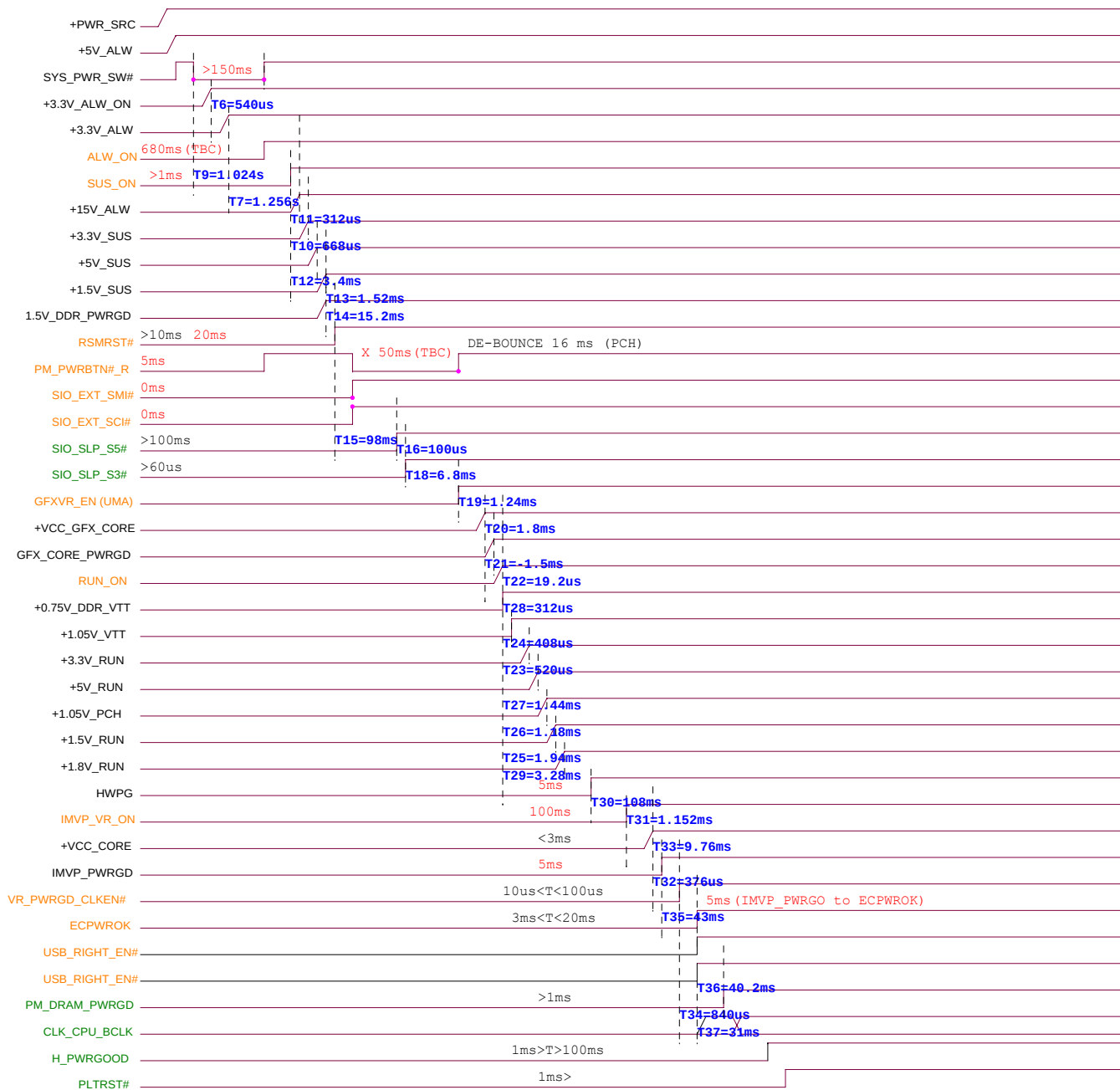
Size	Document Number	Rev
	Batt & DC-IN	1A
Date:	Wednesday, February 10, 2010	Sheet 41 of 44

www.vinafix.vn





UM8_X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



Power Design Block Diagram

